General Description

The PIS2200 is a versatile controller designed for use in Boost, SEPIC and power converter and topologies that needs an external low-side N-MOSFET acting as primary switch. Besides cycle-by-cycle current limiting, current mode control scheme also makes it wide bandwidth and good transient response. The current limit can be programmed simply with an external resistor.

The switching frequency can be set in any value between 100kHz and 1MHz with a resistor or any external clock source. The PIS2200 can be operated at high switching frequency to save the solution board size. While entering shutdown mode, the PIS2200 only sinks 5μA and it allows power supply sequencing. It has built-in protection circuits such as thermal shutdown, under-voltage lockout, short circuit protection, and overvoltage protection. Internal soft-start circuitry reduces the inrush current at start-up.

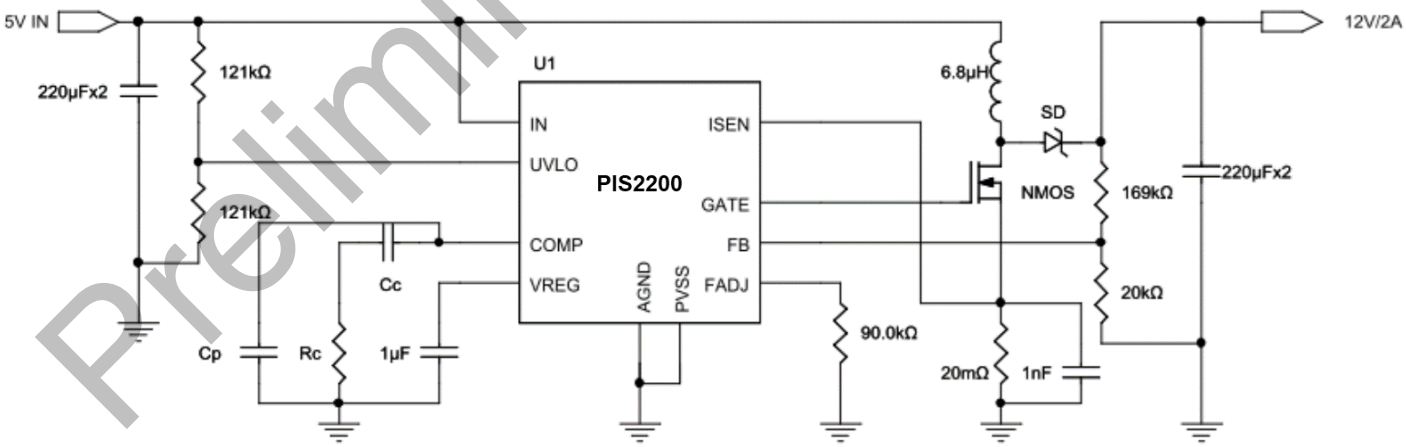
Features

- *Wide Input Voltage from 2.97V to 40V*
- *Reference Voltage with ±3% Accuracy*
- *Adjustable 100kHz~1MHz Clock Frequency*
- *10μA Shutdown Current*
- *1A Peak Current Limit Using Internal Driver*
- *Current Mode Operation*
- *Internal 4/2Ω MOSFET Switch*
- *External RC Compensation*
- *Internal Soft-Start*
- *High Efficiency at Light Loads*
- *Current Limit and Over Temperature Protection*
- *Adjustable Input UVLO Threshold Voltage*

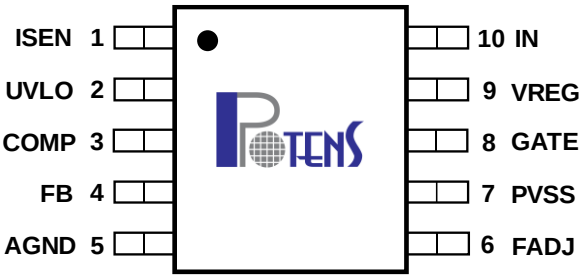
Applications

- *Portable Speakers*
- *Offline Power Supply*
- *Battery Powered Device*
- *Set-Top Box*
- *Photovoltaic Inverters*

Typical Applications



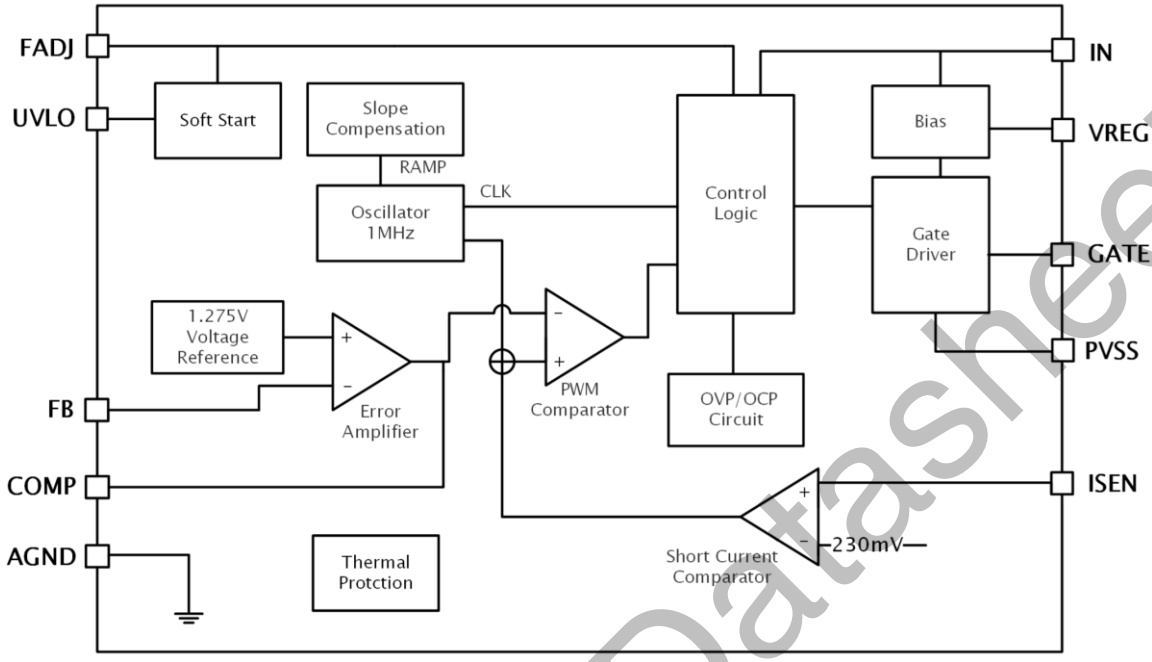
MSOP10 Pin Configuration



Top View

Pin No.	Symbol	I/O/P	Function
1	ISEN	P	Current Sense. Use an external resistor in series with ground to measure the voltage
2	UVLO	I	Under Voltage Lockout. Use a proper ratio resistor divider network to determine the voltage input to allow switching and the hysteresis to disable switching.
3	COMP	I	Compensation. Use a RC/C network to do proper loop compensation.
4	FB	I	Output Feedback. Connect the external resistor divider network from output to this pin to sense output voltage. The FB pin voltage is regulated to internal 1.275V reference voltage.
5	AGND	P	Analog Ground. Connect to exposed pad.
6	FADJ	I	Frequency Adjust/Synchronization/Shutdown. A resistor connected from this pin to ground simply sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the clock. Pull on this pin for ≥ 30 μs will turn the device off and the device will then very few current about 5μA from the supply.
7	PVSS	I	Power Ground. Connect to exposed pad.
8	GATE	O	Gate Drive. Connect this terminal to the gate pin of the external MOSFET.
9	VREG	O	Drive Supply Voltage. A bypass capacitor must be connected from this pin to ground. Do not bias this pin with external power source.
10	IN	I	Power Supply Input.

Functional Block Diagram



Absolute Maximum Ratings (T_a=25 ℃, unless otherwise noted)

Symbol	Parameter	Min	Max	Units
V_{IN}	Supply voltage range	-0.3	42	V
V_{LV} (COMP/UVLO/FB/FADJ/GATE)	Low voltage range	-0.3	6	V
V_{CC}(VREG)	Regulator output pin range	-0.3	5	V
V_{ISEN}	Current sense pin range	-0.4	0.6	V
T_J	Operating junction temperature range	-40	150	˚C
T_{STG}	Storage temperature range	-65	150	˚C
Electrostatic discharge	Human body model	---	2	kV
Electrostatic discharge	Machine model	---	200	V
$\theta_{JC(top)}$	Thermal resistance (Junction to Case $_{(top)}$)	---	46	˚C/W
θ_{JA}	Thermal resistance (Junction to Air)	---	147	˚C/W
θ_{JB}	Thermal resistance (Junction to Board)	---	81	˚C/W
Ψ_{JT}	Junction-to-top characterization parameter	---	3	˚C/W
Ψ_{JB}	Junction-to-board characterization parameter	---	77	˚C/W

* Stress beyond those listed at “absolute maximum rating” table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up “recommended operation conditions” table.

Recommend Operating Condition

Symbol	Parameter	Min	Max	Units
V_{IN}	Supply voltage range	2.97	40	V
f_{OSC}	Switching Frequency range	0.1	1	MHz
T_J	Operating junction temperature range	-40	125	˚C

Electrical Characteristic

(V_{IN}=12V, R_{FADJ}=150kΩ, T_a=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{FB}	Feedback voltage	V_{COMP}=1.4V, 3V<V_{IN}<40V	---	1.275	---	V
		V_{COMP}=1.4V, 3V<V_{IN}<40V -40℃<T_J<125℃	1.236	---	1.313	
I_Q	Quiescent current in shutdown mode	V_{FADJ}=3V, V_{IN}=12V	---	10	---	μA
		V_{FADJ}=3V, V_{IN}=12V -40℃<T_J<125℃	---	---	15	
		V_{FADJ}=3V, V_{IN}=5V	---	5	---	
		V_{FADJ}=3V, V_{IN}=5V, -40℃<T_J<125℃	---	---	10	
V_{UVLO}	Under voltage lockout	V_{UVLO} Ramp down	1.345	---	1.517	V
I_{UVLO}	UVLO source current	Enabled	---	4.5	---	μA
V_{UVLOSD}	UVLO Shutdown voltage		0.55	0.7	0.82	V
V_{COMP}	COMP pin voltage	V_{FB} = 1.275V	---	1	---	V
$R_{DS(ON)}$	High-side switch RDS(ON)	V_{IN}=5V, I_{GATE}=0.2A	---	4	---	Ω
	Low-side switch RDS(ON)	V_{IN}=5V, I_{GATE}=0.2A	---	2	---	
A_{VOL}	Error amplifier voltage gain	V_{COMP}=1.4V, I_{EAO}=100μA	---	60	---	V/V
g_M	Error amplifier trans-conductance	V_{COMP}=1.4V	---	430	---	μS
V_{GATE}	Maximum GATE driving swing	V_{IN} < 5.8V	---	V_{IN}	---	V
		V_{IN} ≥ 5.8V	---	5.2	---	
f_{OSC}	Oscillation frequency	R_{FADJ}=150kΩ	---	0.146	---	MHz
		R_{FADJ}=150kΩ ,-40℃<T_J<125℃	0.125	---	0.2	
D_{MAX}	Maximum duty cycle	R_{FADJ}=150kΩ	---	85	---	%
ΔV_{LINE}	Voltage line regulation	3V<V_{EN}<40V	---	0.02	---	%/V
ΔV_{LOAD}	Voltage load regulation	I_{EAO} Source/Sink	---	±0.5	---	%/A
$t_{MIN(ON)}$	Minimum on-time		---	---	571	ns
I_{SUPPLY}	Supply Current	R_{FADJ}=150kΩ	---	3.3	---	mA
		R_{FADJ}=150kΩ ,-40℃<T_J<125℃	---	---	5	
V_{SENSE}	Current sense threshold voltage	V_{IN} = 12V	---	160	---	mV
		V_{IN} = 12V , -40℃<T_J<125℃	120	---	200	
V_{SC}	Overload current limit sense voltage	V_{IN} = 12V	---	200	---	mV
		V_{IN} = 12V , -40℃<T_J<125℃	160	---	350	
V_{SL}	Internal compensation ramp		---	90	---	mV

Electrical Characteristic – cont.

(V_{IN}=12V, R_{FADJ}=150kΩ, T_a=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OVP}	Output overvoltage protection	V_{COMP} = 1.4V	26	85	135	mV
$V_{OVP(HYS)}$	Output overvoltage protection hysteresis	V_{COMP} = 1.4V	28	70	106	mV
I_{EAO}	Error amplifier output current (Source/Sink)	Source, V_{COMP} = 1.4V, V_{FB} = 0V	---	650	---	μA
		Source, V_{COMP} = 1.4V, V_{FB} = 0V, -40℃<T_J<125℃	470	---	950	
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V	---	57	---	
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V, -40℃<T_J<125℃	30	---	105	
V_{EAO}	Error amplifier output voltage	Upper Limit : V_{FB}=0V, COMP pin floating	---	2.65	---	V
		Upper Limit : V_{FB}=0V, COMP pin floating -40℃<T_J<125℃	2.4	---	2.95	
		Lower Limit : V_{FB} = 1.4V	---	0.65	---	
		Lower Limit : V_{FB} = 1.4V, -40℃<T_J<125℃	0.32	---	0.9	
V_{SD}	Shutdown signal threshold on FADJ pin*	Output = High Level (SD)	---	1.26	---	V
		Output = High Level (SD), -40℃<T_J<125℃	---	---	1.4	
		Output = Low Level (EN)	---	0.63	---	
		Output = Low Level (EN), -40℃<T_J<125℃	---	---	0.4	
t_{SS}	Soft start delay	V_{FB} = 1.2V, COMP pin floating	8.7	15	21.3	ms
t_R	GATE pin rising time	Cgs = 3000pF, V_{GATE} = 0V to 3V	---	18	---	ns
t_F	GATE pin falling time	Cgs = 3000pF, V_{GATE} = 3V to 0V	---	12	---	ns
I_{SD}	Shutdown pin current FADJ pin	V_{SD}=0V	---	10	---	μA
T_{SD}	Thermal shutdown		---	175	---	℃
$T_{SD(HYS)}$	Thermal shutdown hysteresis		---	10	---	℃

* The FADJ pin should be pulled to VIN through a resistor to turn the regulator off. The voltage on the FADJ pin must be above the maximum limit for Output = High Level to keep the regulator off and must be below the limit for Output = Low Level to keep the regulator on.

Functional Descriptions

The PIS2200 employs the current-mode, adjustable frequency pulse-width modulation (PWM) architecture. It operates at adjustable switching frequency under medium to high load current conditions.

Overvoltage and UVLO Protection

The PIS2200 uses FB pin to detect overvoltage occurrence. The overvoltage protection should be triggered at the voltage rises to $V_{FB}+V_{OVP}$. When OVP occurs only the MOSFET will be turned off, the output voltage will drop. PIS2200 will switch when the voltage on FB pin is less then ($V_{OVP}+V_{FB}-V_{OVP(HYS)}$).

The PIS2200 provides UVLO pin to program enable and disable thresholds. The voltage on UVLO pin would be compared with internal reference 1.43V. Figure 1 shows how the UVLO detection works.

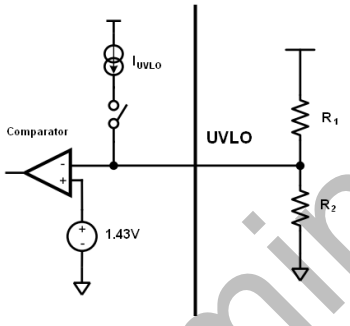


Figure 1. UVLO Pin Configuration

The R1/R2 network programs the enable threshold voltage V_{EN}. When the PIS2200 is enabled the I_{UVLO} will source 5μA current flows the R_2 which causes a hysteresis. Hence the disable threshold, V_{SH}, is lower then the enable threshold V_{EN}.

$$R_2 = \frac{1.43V}{I_{UVLO}} \times \left(1 + \frac{1.43V - V_{SH}}{V_{EN} - 1.43V}\right)$$

$$R_1 = R_2 \times \left(\frac{V_{EN}}{1.43V} - 1\right)$$

Select appropriate value of V_{EN}, V_{SH} and use above two equations to determine the value of R_1 and R_2.

Bias Voltage

PIS2200 generates the internal bias voltage from IN input voltage if it does not exceeds 6V. When VIN is higher than 6V the PIS2200 will use internal regulation to bias the chip. To improve the stability of the bias, an external capacitor of 0.47μF~4.7μF is strongly recommended to add on VREG terminal.

In any case, do not add external voltage on VREG pin or the chip would be damaged.

Frequency Adjust

The switching frequency can be adjusted from 100kHz to 1MHz by a external resistor in series with FADJ terminal and ground. The following equation is used to calculate resistor value.

a. When Fs < 300KHz the calculate as below,

$$R_{FADJ} \cong \frac{17 \times 10^3}{f_s} + 8.7$$

b. When Fs > 300KHz the calculate as below,

$$R_{FADJ} \cong \frac{21 \times 10^3}{f_s} - 7.2$$

Where f_S is in kHz and R_{FADJ} is in kΩ.

Clock Synchronization

PIS2200 is able to be synchronized to an external clock by connecting to the FADJ terminal with R_{FADJ} in series with ground as shown in figure 2.

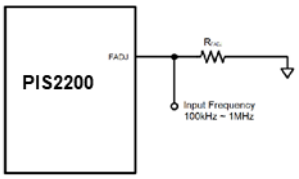


Figure 2. Clock Synchronization

Functional Descriptions (cont.)

Shutdown

The FADJ pin can be used as a shutdown pin. If the high signal pulls up this pin, PIS2200 will stop the switching and then enter the shutdown state. In this state, PIS2200 consumes only 5μA typically.
The use of shutdown control in frequency adjustment mode is quite simple. Connects the FADJ pin to ground will force the PIS2200 runs at specified frequency and pulls this pin high will shutdown the IC. In both frequency and synchronization mode, pulls FADJ pin high lasting then 30μs will also force the PIS2200 enter the shutdown state.

Slope Compensation

PIS2200 employs current mode control scheme. It has many advantages such as cycle-by-cycle current limit for the switch and easier to parallel power stages because automatic current sharing. The compensation ramp is already added in PIS2200 and the slope of the default compensation ramp could satisfy most applications.

Overvoltage Protection

The PIS2200 has overvoltage protection for the output. OVP occurrence is detected by sensing feedback (FB) pin. When the voltage at FB pin is over $V_{FB}+V_{OVP}$, overvoltage protection is triggered and the drive pin and the GATE pin will be tied-low.

Once the voltage at FB pin is lower than $V_{FB}+(V_{OVP}-V_{OVP(HYS)})$, the PIS2200 will begin to switch again. Be aware that the error amplifier is still in operation during OVP event.

Short Circuit Protection

The ISEN pin is used to sense the over-current occurrence. If the difference between ISEN pin and ground is greater than 230mV, the current limit will be activated. The comparator will decrease the switching frequency by the factor of 8 and maintains this condition until the over-current (short) event is removed.

Application Information

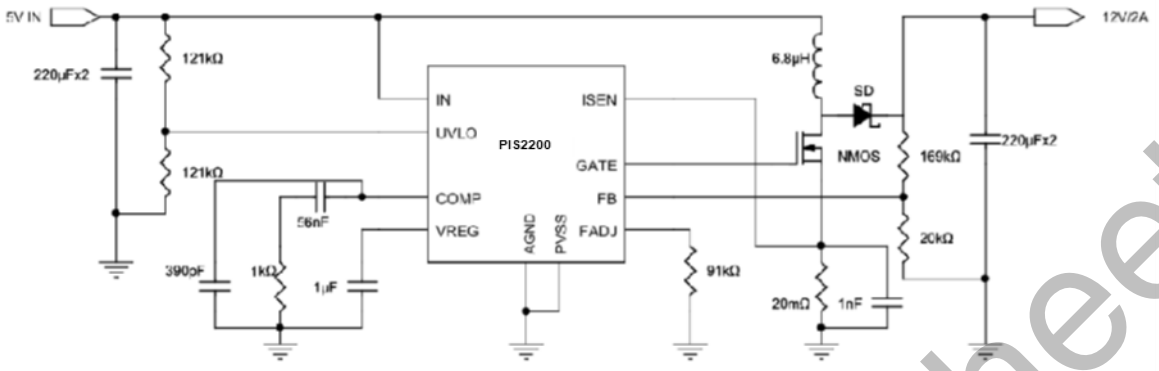


Figure 3 PIS2200 Typical Boost Application

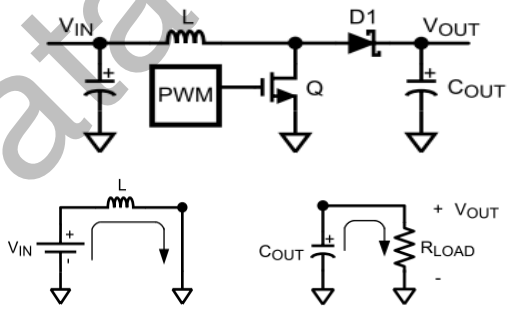
The most common topology for the PIS2200 is the boost or step-up topology. The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost regulator is shown in Figure 4. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles. In the first cycle of operation, MOSFET Q is turned on and energy is stored in the inductor. During this cycle, diode D1 is reverse biased and load current is supplied by the output capacitor, C_{OUT}. In the second cycle, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined as:

$$V_{OUT} = \frac{V_{IN}}{1-D}$$

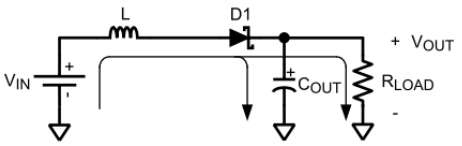
(ignoring the voltage drop across the MOSFET and the diode), or

$$V_{OUT} + V_{D1} - V_Q = \frac{V_{IN} - V_Q}{1-D}$$

where D is the duty cycle of the switch, V_{D1} is the forward voltage drop of the diode, and V_Q is the drop across the MOSFET when it is on. The following sections describe selection of components for a boost converter.



A. First Cycle of Operation



B. Second Cycle of Operation

Figure 4. Simplified Boost Converter Diagram

Power Inductor Selection

The inductor is one of the two energy storage elements in a boost converter. Figure 5 shows how the inductor current varies during a switching cycle. The current through an inductor is quantified as:

$$V_L(t) = L\frac{di_L(t)}{dt}$$

Application Information (cont.)

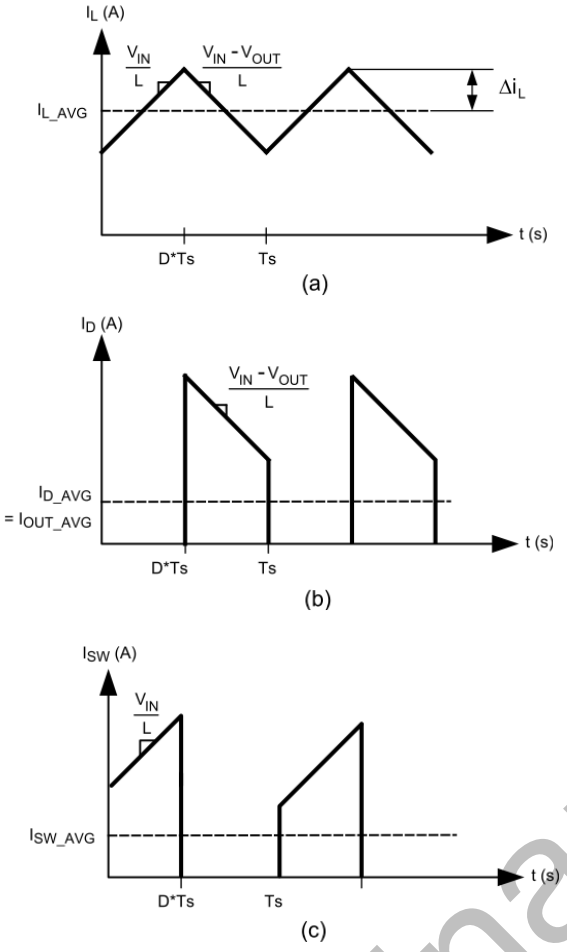


Figure 5. (a) Inductor Current (b) Diode Current (c) Switch Current

If $V_L(t)$ is constant, $di_L(t)/dt$ must be constant. Hence, for a given input voltage and output voltage, the current in the inductor changes at a constant rate.

The important quantities in determining a proper inductance value are I_L (the average inductor current) and Δi_L (the inductor current ripple difference between the peak inductor current and the average inductor current). If Δi_L is larger than I_L , the inductor current drops to zero for a portion of the cycle and the converter operates in discontinuous conduction mode. If Δi_L is smaller than I_L , the inductor current stays above zero and the converter operates in continuous conduction mode. All the analysis in this data sheet assumes operation in continuous conduction mode. To operate in continuous conduction mode, the following conditions must be met:

(1) $$I_L > \Delta i_L$$

(2) $$\frac{I_{OUT}}{1-D} > \frac{DV_{IN}}{2 f_S L}$$

(3) $$L > \frac{D(1-D)V_{IN}}{2 I_{OUT} f_S}$$

Choose the minimum I_{OUT} to determine the minimum L. A common choice is to set (2 x Δi_L) to 30% of I_L . Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter,

(4) $$I_L = \frac{I_{OUT}}{1-D}$$

(5) $$I_{L\_PEAK} = I_L(\max) + \Delta i_L(\max)$$

(6) $$\Delta i_L = \frac{DV_{IN}}{2 \times L \times f_S}$$

A core size with ratings higher than these values should be chosen. If the core is not properly rated, saturation will dramatically reduce overall efficiency.

The PIS2200 can be set to switch at very high frequencies. When the switching frequency is high, the converter can operate with very small inductor values. With a small inductor value, the peak inductor current can be extremely higher than the output currents, especially under light load conditions.

Application Information (cont.)

The PIS2200 senses the peak current through the switch. The peak current through the switch is the same as the peak current calculated above.

Programming the Output Voltage and Output Current

The output voltage can be programmed using a resistor divider between the output and the feedback pins, as shown in Figure 6. The resistors are selected such that the voltage at the feedback pin is 1.275V. R_{F1} and R_{F2} can be selected using the equation,

$$V_{OUT} = 1.275(1 + \frac{R_{F1}}{R_{F2}})$$

A 100pF capacitor may be connected between the feedback and ground pins to reduce noise.

The maximum amount of current that can be delivered at the output can be controlled by the sense resistor, R_{SEN} . Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage, V_{SENSE} . Limits for V_{SENSE} have been specified in the Electrical Characteristics section. This can be expressed as:

$$I_{SW(pexk)} \times R_{SEN} = V_{SENSE} - D \times V_{SL}$$

The peak current through the switch is equal to the peak inductor current.

$$I_{SW(pexk)} = I_L(\max) + \Delta i_L$$

Therefore for a boost converter,

$$I_{SW(pexk)} = \frac{I_{OUT(\max)}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_s \times L)}$$

Combining the two equations yields an expression for R_{SEN} ,

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SL})}{\left[\frac{I_{OUT(\max)}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)}\right]}$$

Evaluate R_{SEN} at the maximum and minimum V_{IN} values and choose the smallest R_{SEN} calculated.

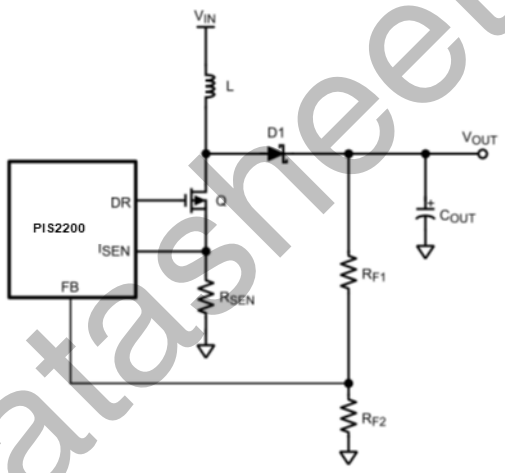


Figure 6. Adjusting the Output Voltage

Application Information (cont.)

Power Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than the inductor peak current. The peak diode current can be calculated using the formula:

$$I_{D(Peak)} = \left[I_{OUT}/(1-D)\right] + \Delta i_L$$

I_{OUT} is the output current and Δi_L has been defined in Figure 5. The peak reverse voltage for a boost converter is equal to the regulator output voltage. The diode must be capable of handling this peak reverse voltage. To improve efficiency, a low forward drop Schottky diode is recommended.

Power MOSFET Selection

The drive pin, DR, of the PIS2200 must be connected to the gate of an external MOSFET. In a boost topology, the drain of the external N-Channel MOSFET is connected to the inductor and the source is connected to the ground. The drive pin voltage, V_{DR} , depends on the input voltage. In most applications, a logic level MOSFET can be used. For very low input voltages, a sub-logic level MOSFET should be used.

The selected MOSFET directly controls the efficiency. The critical parameters for selection of a MOSFET are:

- Minimum threshold voltage, $V_{TH(MIN)}$
- On-resistance, $R_{DS(ON)}$
- Total gate charge, Q_g
- Reverse transfer capacitance, C_{RSS}
- Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage. $V_{DS(MAX)}$ of the MOSFET must be greater than the output voltage. The power losses in the MOSFET can be categorized into conduction losses and ac switching or transition losses. $R_{DS(ON)}$ is needed to estimate the conduction losses. The conduction loss, P_{COND} , is the I^2R loss across the MOSFET. The maximum conduction loss is given by:

$$P_{COND(MAX)} = \left(\frac{I_{OUT(\max)}}{1-D_{MAX}}\right)^2 \times D_{MAX} \times R_{DS(ON)}$$

where D_{MAX} is the maximum duty cycle.

$$D_{MAX} = \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)$$

At high switching frequencies the switching losses may be the largest portion of the total losses.

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often, the individual MOSFET datasheet does not give enough information to yield a useful result. As below equation give a rough idea how the switching losses are calculated:

$$P_{SW} = \frac{I_{L\max} \times V_{out}}{2} \times f_{SW} \times (t_{LH} + t_{HL})$$

$$t_{LH} = \left(Qgd + \frac{Qgs}{2}\right) \times \frac{R_{Gate}}{V_{DR} - Vgs_{th}}$$

Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular, as shown in Figure 5. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta i_L / \sqrt{3} = \left(\frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times L \times f_S}\right)$$

The input capacitor should be capable of handling the rms current. Although the input capacitor is not as critical in a boost application, low values

Application Information (cont.)

can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 100µF to 200µF. If a value lower than 100µF is used, then problems with impedance interactions or switching noise can affect the PIS2200. To improve performance, especially with V_{IN} below 8 V, it is recommended to use a 20Ω resistor at the input to provide a RC filter. This resistor is placed in series with the V_{IN} pin with only a bypass capacitor attached to the V_{IN} pin directly (see Figure 7). A 0.1µF or 1µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

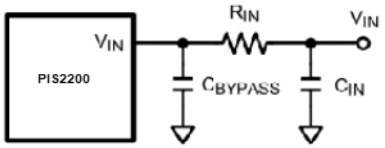


Figure 7 Reducing IC Input Noise

Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the inductor is charging. As a result it sees very large ripple currents. The output capacitor should be capable of handling the maximum rms current. The rms current in the output capacitor is:

$$I_{CIN(RMS)} = \sqrt{(1-D)\left[I_{OUT^2}\frac{D}{(1-D)^2} + \frac{\Delta i_L{}^2}{3}\right]}$$

Where

$$\Delta i_L = \frac{DV_{IN}}{2 \times L \times f_S}$$

and D, the duty cycle is equal to (V_{OUT} − V_{IN})/V_{OUT}.

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo- OSCON, or multi-layer ceramic capacitors are recommended at the output.

Driver Supply Capacitor Selection

A good quality ceramic bypass capacitor must be connected from the V_{CC} pin to the PGND pin for proper operation. This capacitor supplies the transient current required by the internal MOSFET driver, as well as filtering the internal supply voltage for the controller. A value of between 0.47µF and 4.7µF is recommended.

Application Information (cont.)

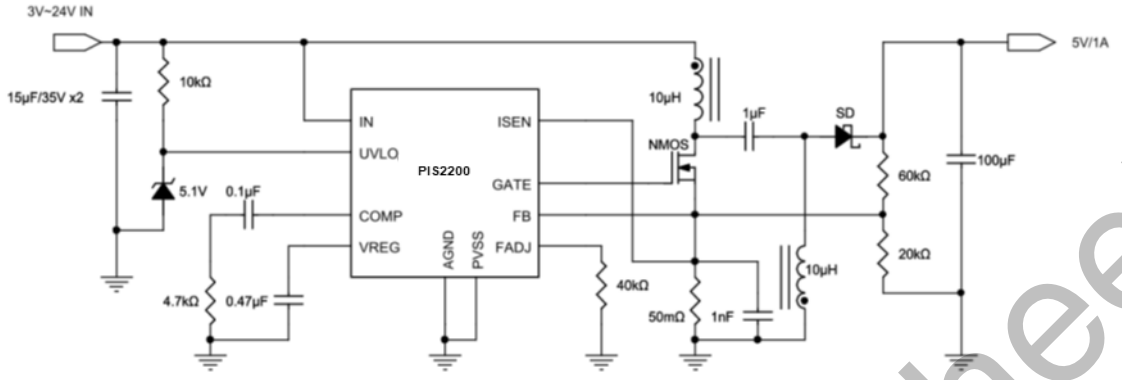


Figure8 PIS2200 Typical SEPIC Application

PIS2200 can also be used in SEPIC application because of it controls low-side of NMOSFET. Figure 8 shows the PIS2200 typical SEPIC application. This configuration allows the input voltage higher or lower then output voltage. For both stepping-up and stepping-down configuration, two inductors are needed. The two inductors can be individual inductor or two windings of a coupled transformer. For reducing input ripple it is better to use the coupled windings of transformers for both inductors.

The advantage of SEPIC structure over a boost converter is input and output isolation. The input and the output of pure boost converter is always connected through an inductor unless external switch is added. For SEPIC structure, a capacitor isolates the input from the output and provides protection against shorted or malfunctioning load. Hence, the SEPIC is useful for replacing boost circuits when true shutdown is required. This means that the output voltage falls to 0V when the switch is turned off. In pure boost converter, the output can only fall to the input voltage minus a diode drop and never turn off the output.

To properly pick up the components for the application, the following parameters need to be examined

Input voltage range, output voltage, output current range and the switching frequency. These four main parameters will affect the operating characteristic of the application.

MOSFET Selection

Four parameters will dominate the selection of the MOSFET: minimum threshold voltage $V_{TH(MIN)}$, the On-resistance $R_{DS(ON)}$, the total gate charge Qg, the reverse transfer capacitance Css and the maximum drain to source voltage $V_{DS(MAX)}$.

The peak switch voltage in SEPIC application is:

$$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_{DIODE}$$

Hence the VDS(MAX) of MOSFET shell be:

$$V_{DS(MAX)} > V_{SW(PEAK)}$$

The peak switch current is determined by:

$$I_{SW(PEAK)} = I_{L1(AVG)} + I_{OUT} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2}$$

Where ΔI_{L1} and ΔI_{L2} are the peak-to-peak ripple currents of the inductors respectively.

The RMS current through the switch is given by:

$$I_{SW(RMS)} = \sqrt{\left[I_{SW(PEAK)}{}^2 - I_{SW(PEAK)}(\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3} \right] D}$$

Application Information (cont.)

Power Diode Selection

The diode must be selected to handle the peak current and the peak reverse voltage. In SEPIC application, the diode peak current is the same as the switch peak current. The off-state voltage or peak reverse voltage of the diode is $V_{IN}+V_{OUT}$. Similar to the boost converter, the average diode current is equal to the output current. In order to improve the efficiency, schottky diodes are recommended.

Inductor Selection

The inductors shall be chosen carefully to satisfy constant current mode requires calculations of the following parameters:

Inductor average current:

$$I_{L1(AVG)} = \frac{D \times I_{OUT}}{1-D}$$

$$I_{L2(AVG)} = I_{OUT}$$

Peak-to-peak ripple current:

$$\Delta I_{L1} = \frac{D \times (V_{IN} - V_Q)}{f_S \times L_1}$$

$$\Delta I_{L2} = \frac{D \times (V_{IN} - V_Q)}{f_S \times L_2}$$

Maintaining the condition $I_L > \Delta I_L/2$ to ensure continuous conduction mode yields the following minimum values for L_1 and L_2:

$$L_1 > \frac{(1-D) \times (V_{IN} - V_Q)}{f_S \times I_{OUT} \times 2}$$

$$L_2 > \frac{D \times (V_{IN} - V_Q)}{f_S \times I_{OUT} \times 2}$$

Peak current in the inductor, to ensure the inductor does not saturate:

$$I_{L1(PK)} = \frac{D \times I_{OUT}}{1-D} + \frac{\Delta I_{L1}}{2}$$

$$I_{L2(PK)} = I_{OUT} + \frac{\Delta I_{L2}}{2}$$

$I_{L1(PK)}$ must be lower than the maximum current rating set by the current sense resistor.

The value of L1 can be increased above the minimum recommended value to reduce input ripple and output ripple. However, once ΔI_{L1} is less than 20% of $I_{L1(AVG)}$, the benefit to output ripple is minimal.

By increasing the value of L2 above the minimum recommendation, ΔI_{L2} can be reduced, which in turn will reduce the output ripple voltage:

$$\Delta V_{OUT} = \left(\frac{I_{OUT}}{1-D} + \frac{\Delta I_{L2}}{2} \right) \times ESR$$

where ESR is the equivalent series resistance of the output capacitor.

If L1 and L2 are wound on the same core, then L1=L2=L. All the equations above will hold true if the inductance is replaced by 2L.

Input Capacitor Selection

Like boost structure, SEPIC has an inductor at the input. The inductor ensures that the input capacitor sees fairly low ripple currents and the capacitor should be capable of handling the input RMS current. In SEPIC application, lower values can cause impedance interactions. Therefore a good quality capacitor such as polymer tantalum, OS-con or multilayer ceramic capacitors is recommended in the range from 100µF to 200µF.

To improve the performance especially when V_{IN} is under 8V, the input RC low pass filter could be added. Refer the input capacitor selection in boost controller application for details.

Application Information (cont.)

Output Capacitor Selection

The output capacitors directly affect the output ripple. Use capacitors with low ESR and ESL at the output for higher efficiency and lower ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, OS-Con, or multi-layer ceramic capacitors are recommended at the output for low ripple.

Resistor Selection

The peak current through the MOSFET, $I_{SW(PEAK)}$, can be adjusted using the current sense resistor, R_{SEN} , to limit at certain output current. R_{SEN} can be selected using the following equation:

$$R_{SEN} = \frac{V_{SENSE} - D \times (V_{SL} + \Delta V_{SL})}{I_{SW(PEAK)}}$$

Isolation Capacitor Selection

The isolation capacitor C_S , depends on the rms current. The rms current of the SEPIC capacitor is given by:

$$I_{CSRMS} = \sqrt{I_{SWRMS}^{\ 2} + (I_{L1PK}^{\ 2} - I_{L1PK}\Delta I_{L1} + \Delta I_{L1}^{\ 2})(1-D)}$$

The isolation capacitor must be rated for a large ACrms current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the rms current through the capacitor is small (relative to capacitor technology). The voltage rating of the isolation capacitor must be greater than the maximum input voltage. Tantalum capacitors are the best choice for SMT, having high rms current ratings relative to size. Ceramic capacitors could be used, but the low C values will tend to cause larger changes in voltage across the capacitor due to the large currents, and high C value ceramics are expensive.

Electrolytics work well for through hole applications where the size required to meet the rms current rating can be accommodated. There is an energy balance between C_S and L1, which can be used to determine the value of the capacitor. The basicenergy balance equation is:

$$\frac{1}{2} C_S \Delta V_S^{\ 2} = \frac{1}{2} (L1) \Delta I_{L1}^{\ 2}$$

Where

$$\Delta V_S = \left(\frac{V_{OUT}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}}\right) \times \frac{I_{OUT}}{f_S C_S}$$

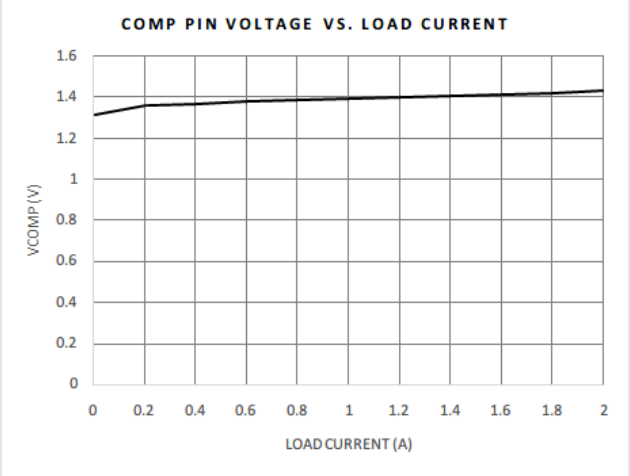
is the ripple voltage across the isolation capacitor, and

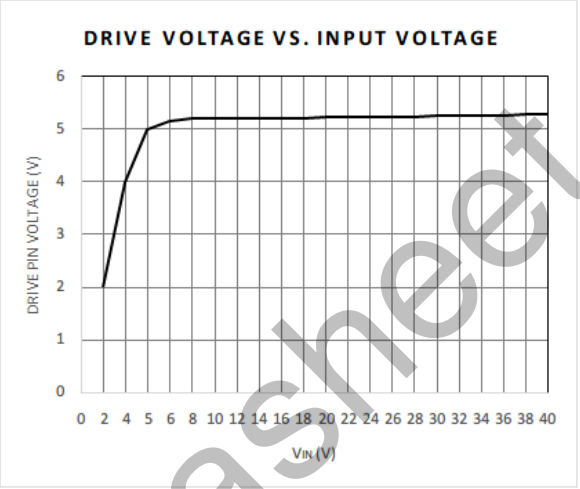
$$\Delta I_{L1} = \frac{(V_{IN} - V_Q) \times D}{(L1)\, f_S}$$

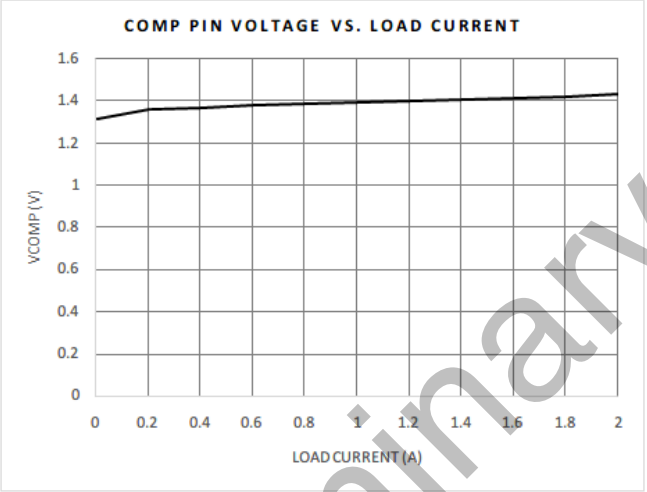
is the ripple current through the inductor L1. The energy balance equation can be solved to provide a minimum value for Cs :

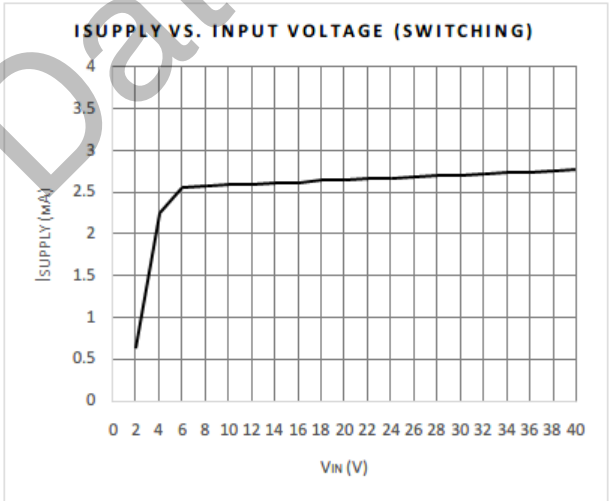
$$C_S \geq L1 \frac{I_{OUT}^{\ 2}}{(V_{IN} - V_O)^2}$$

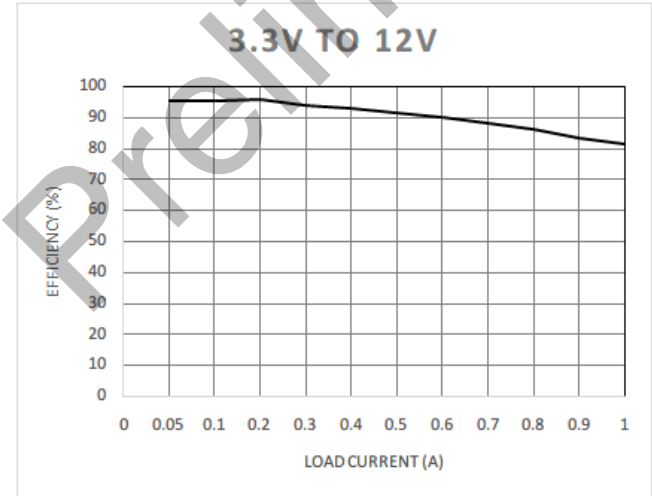
Typical Characteristic (cont.)

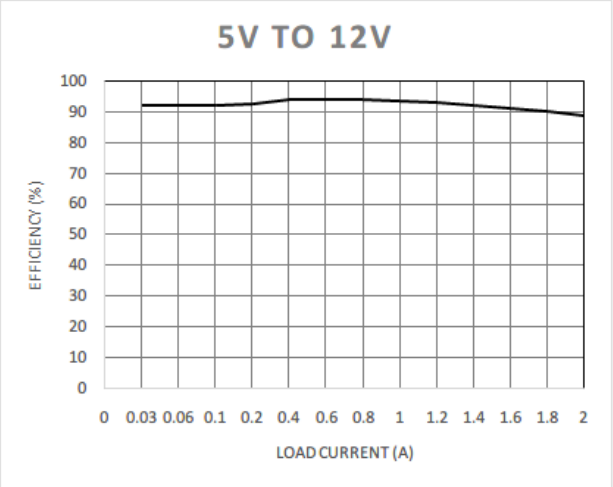












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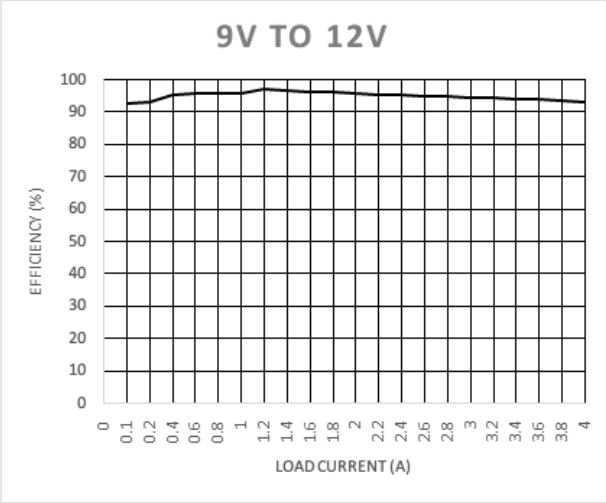

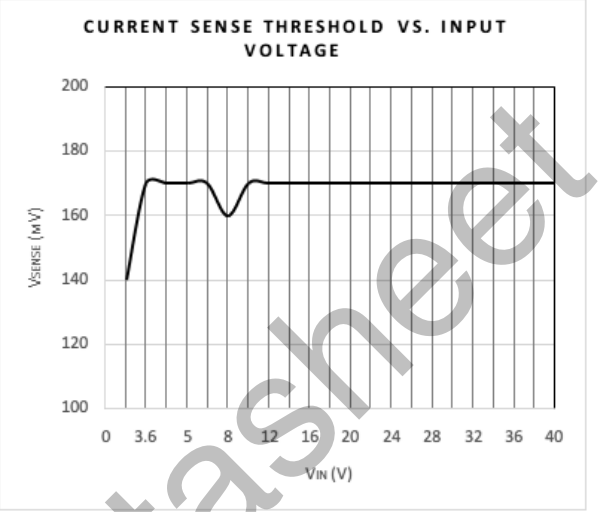

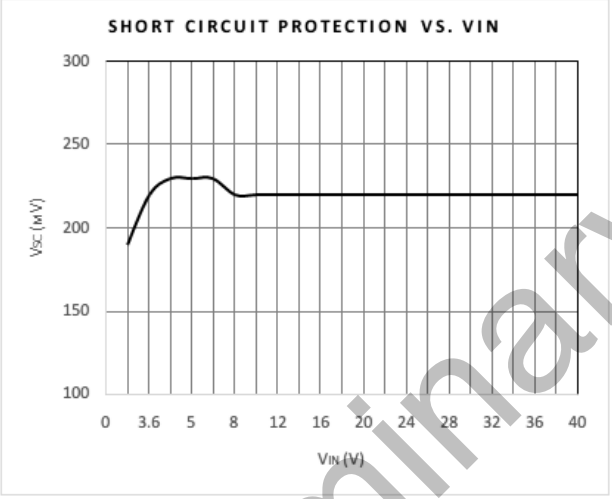

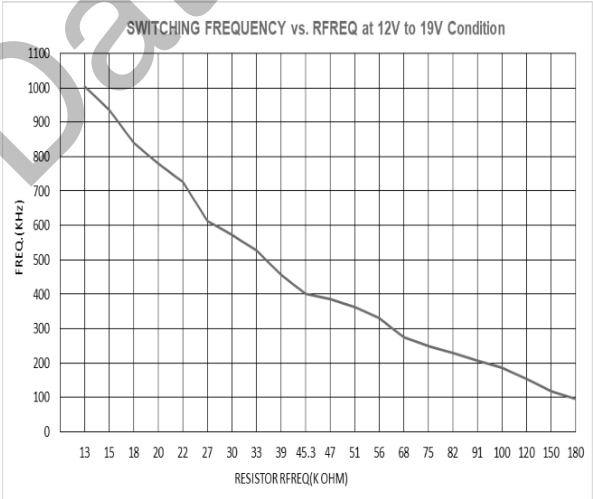

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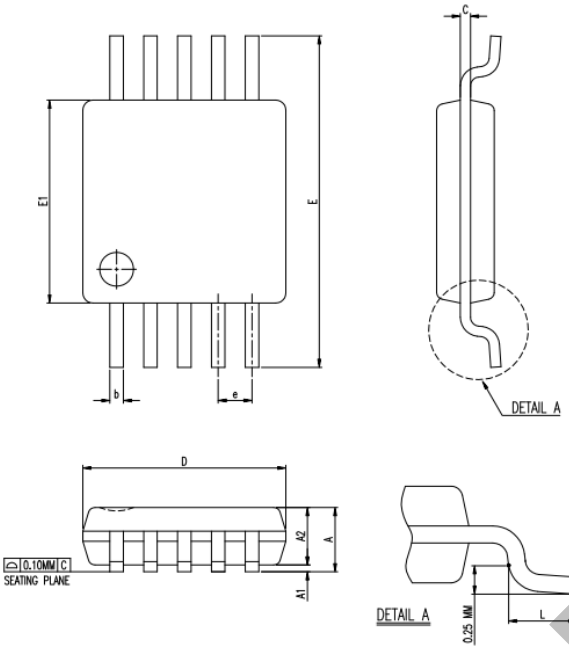

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	1.02	1.10	0.032	0.040	0.043
A1	0.05		0.15	0.002		0.006
A2	0.75	0.86	0.95	0.030	0.034	0.037
b	0.17	0.20	0.27	0.007	0.008	0.011
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	0.50 BASIC			0.020 BASIC		
L	0.40	0.55	0.70	0.016	0.022	0.028
θ	0°	3°	6°	0°	3°	6°
JEDEC						

NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH ,
TIE BAR BURRS AND GATE BURRS
MOLD FLASH , TIE BAR BURRS AND GATE BURRS SHALL NOT
EXCEED 0.005 INCH (0.12 MM) PER END DIMENSION " E1 "
DOES NOT INCLUDE INTERLEAD FLASH.
INTERLEAD FLASH SHALL NOT EXCEED 0.010 INCH (0.25 MM)
PER SIDE .