1. Description

The PID3190A are high-performance Smart Power Stage (SPS) with 90A peak current capability. They contain high-side and low-side N-Channel MOSFETs and a synchronous buck driver IC. The driver IC integrates high accuracy current sense, temperature sense, comprehensive protection mechanism.

The PID3190A internal current sense is based on drain source voltage (VDS) of both high-side and low-side MOSFET current, using algorithm with temperature compensation and inductance calibration to achieve superior current sense accuracy and lower propagation delay. Protections include cycle-by-cycle over current protection with programmable thresholds, VCC/VDRV UVLO protection, phase fault detection, IC temperature reporting and thermal shutdown. Operation frequency is up to 1.2MHz at steady state and 4MHz at transient state, providing high performance transient response.

The PID3190A are offered in 5mm x 6mm DFN package, which is optimized for high−current application and can greatly reduce parasitic and SW ringing, as well as provide excellent heat transfer path.

2. Typical Applications

- High current, high frequency DC-DC converters
- Voltage Regulators for CPUs, GPUs, and DDR memory arrays of Desktop & Notebook Microprocessors
- Routers, Switches and other ASICs

3. Features

- Internal high accuracy and low delay current sense
- 30V(HS)/25V(LS) breakdown voltage of MOSFETs for higher robustness reliability
- Operating frequency up to 1.2MHz for steady state, 4MHz for transient state
- Peak output current capability up to 90A
- Responds properly to Tri-state PWM input
- Precise output current monitoring of 5μA/A
- Precise temperature monitoring of 8mV/℃
- Support switch node fault detection and flag
- Cycle-by-cycle over current protection
- OCP and thermal shutdown with fault flag
- 5mm x 6mm x 0.9mm DFN-39 package
- Catastrophic Fault Detection
  a. Over−temperature Protection
  b. Over-current protection (POCP & NOCP)
  c. UVLO on VCC and VDRV
  d. High-side and low-side MOSFET short
  e. UVLO on BOOT-PHASE

4. Application Diagram

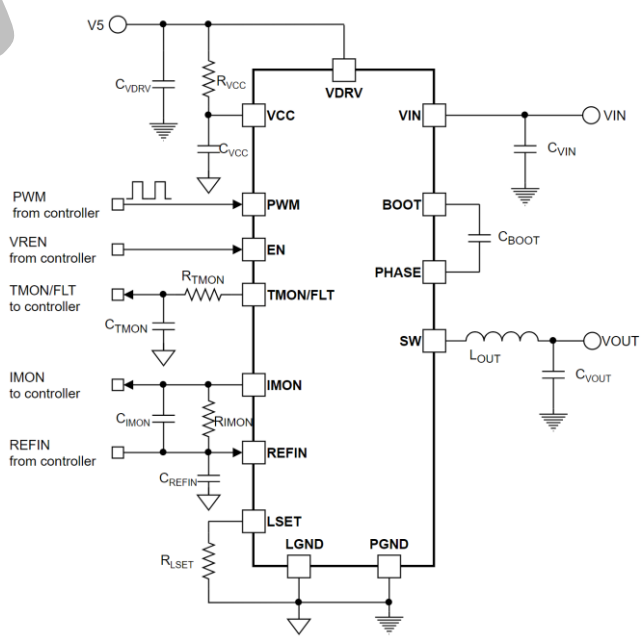


Figure 1. Typical Application Diagram

5. Order Information

Part Number	Package Type	Package Qty	MSL	POCP
PID3190A	DFN5X6-39L	5000	1	120A

6. Package Reference and Pin Functions

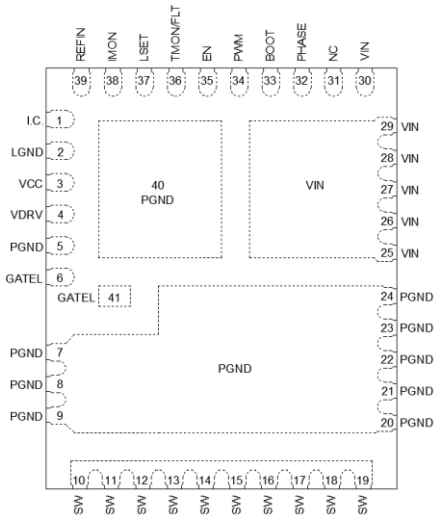


Figure 2. DFN5X6-39L Package(Top View)

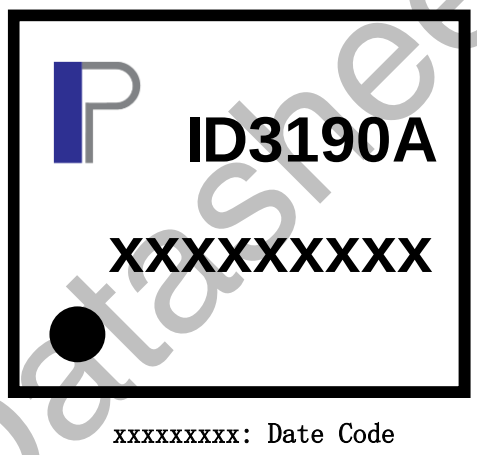


Figure 3. PID3190A Top Marking

Pin #	Name	Description
1	I.C.	Internal connection, can be left floating or connected to VOUT.
2	LGND	Signal ground. All signals are referenced to this pin.
3	VCC	Bias voltage for control logic. Connect a X7R 1μF ceramic capacitor between VCC and LGND and a 1Ω resistor between VCC and VDRV pins.
4	VDRV	The supply of gate driver. Connect a X7R 1μF cap between VDRV and PGND. VDRV should be connected to +5V power supply.
5,7-9, 20-24, 40	PGND	Power ground. It is also the power ground of the low-side MOSFET.
6,41	GATEL	Low-side MOSFET driver pin that can be connected to a test point in order to observe the waveform.
10-19	SW	Switching node of synchronous buck converter.
25-30	VIN	4.5V to 16V high current input voltage connection. Place at least one 1 μF X7R capacitor between VIN pin and PGND pin. Also connect two 10μF X7R /X6S ceramic capacitors in parallel.
31	NC	No connection, leave the pin unconnected or short to VIN.

32	PHASE	Switching node. For bootstrap capacitor connection only.
33	BOOT	Bootstrap capacitor connection. Connect a minimum 0.22 µF X7R ceramic capacitor from BOOT to PHASE pin. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. For applications with VIN greater than 14V, use a 2Ω resistor in series with the bootstrap capacitor to reduce excessive voltage spike at SW node.
34	PWM	3.3V/5V logic level PWM input. PWM input: “High” turns high-side MOSFET on and low-side MOSFET off; “Tri-state” turns both MOSFETs off; “Low” turns the low-side MOSFET on and high-side MOSFET off.
35	EN	Pulling EN high enables the driver; pulling EN low disables the driver and enters ultralow quiescent current mode. Floating this pin is not recommended however a low current pull-down is embedded to keep the driver off if the pin is floating. The EN Pin is VCC tolerant.
36	TMON/FLT	The voltage at this pin is defined by the equation 8mV * (Celsius Temperature) + 0.6V. This pin will be pulled up to 3.3V under severe over temperature, over current, phase fault, BOOT-PHASE UVLO, etc. Refer to Fault Reporting and Identification table for more details. Connect a 10nF decoupling cap between this pin and GND, only 1pcs decoupling cap is needed for multi-phase application.
37	LSET	A resistor from this pin to LGND pin sets the inductor value for the internal current sensing circuitry. 100kΩ for 100nH; Float for 210nH; <10kΩ（or GND）for 120nH. Leave it floating or short to GND if not used this function.
38	IMON	Sensed current output signal referenced to the REFIN pin or a reference voltage. Current on IMON pin represents inductor current information at 5µA/A.
39	REFIN	The reference supply voltage for the IMON information. This pin has a low bias current and can be tied to a fixed voltage between 1.1V and 1.9V such as bias rails from a PWM controller. Use a X7R 0.1µF ceramic capacitor between REFIN and a quiet GND near PWM controller. Can be left floating if not used.

7. Specifications

7.1 Absolute Maximum Ratings Note(1)

		Min	Max	Unit
VIN		–0.3	25	V
VCC, VDRV		–0.3	6	V
SW, PHASE	DC	–0.3	25	V
	Repetitive pulse Note(2)	-5	25	V
VIN-PHASE		-0.3	25	V
	Repetitive pulse Note(2)	-0.3	30	V
BOOT-GND	DC	-0.3	31	V
BOOT-PHASE	DC	–0.3	6	V
All other Pins		–0.3	VCC+0.3	V
	Lead Temperature (Solder)		260	°C
T_J	Virtual junction temperature range	–40	150	°C
T_{STG}	Storage temperature range		150	°C

Notes:

(1) Exceeding these ratings may cause permanent damage to the device

(2) Repetitive pulse ≤15 ns. Verified at bench characterization

7.2 ESD Ratings

			Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 Note(1)	±1	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101 Note(2)	±1	kV

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

7.3 Recommended Operating Conditions

		Min	Max	Unit
VIN		4.5	16	V
VCC, VDRV		4.5	5.5	
REFIN		1.1	1.9	
IMON	IMON Output Range	0.8	VCC-2	V
Fsw		200	1200	kHz
Fsw	During Transient		4000	kHz
Tj		-40	125	°C

Note:

The device is not guaranteed to function outside of its operating conditions.

7.4 Thermal Information

Thermal Metric		Values	Unit
$R_{\theta JA}$	Junction-to-air thermal resistance	21	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	20.4	°C/W
$R_{\theta JC(BOTTOM)}$	Junction-to-case (bot) thermal resistance	0.2	°C/W

8. Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to T_J = 25°C, VCC=VDRV=5V, REFIN = 1.2V, Fsw ≤ 1.2 MHz (unless otherwise specified).

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
PWM						
PWM Input High Threshold	V_{PWM_HI}	PWM Low or Tri-state to High	2.4			V
PWM Input Low Threshold	V_{PWM_LI}	PWM High or Tri-state to Low			0.8	V
Tri-state Voltage Rising Threshold	V_{TRI_HI}	Rising from Tri-state to leaving Tri-state	2.1	2.2	2.3	V
Tri-state Voltage falling Threshold	V_{TRI_LO}	Falling from Tri-state to leaving Tri-state	0.9	1	1.1	V
PWM High Propagation Delay	$t_{DELAY\_PWM\_HI}$	Measured from PWM rising edge to GATEL starts to fall	9.5	14	17	ns
PWM Low Propagation Delay	$t_{DELAY\_PWM\_LO}$	Measured from PWM falling edge to SW starts to fall	23	40	56	ns
Tri-state to High Propagation Delay	$t_{DELAY\_TRI\_HI}$	PWM Tri-state to High transition to SW＞1V	15	21	26	ns
Tri-state to Low Propagation Delay	$t_{DELAY\_TRI\_LO}$	PWM Tri-state to Low transition to GATEL＞1V		11	24	ns
Tri-state Hold Off Time from PWM High	$T_{TRIHOLD\_H2T}$	PWM High to Tri-state transition to SW starts fall	49	61	73	ns
Tri-state Hold Off Time from PWM Low	$T_{TRIHOLD\_L2T}$	PWM Low to Tri-state transition to GATEL starts fall	26	32	38	ns
PWM Input Tri-state Float Voltage	V_{PWM_FLOAT}	PWM Input Floating	1.6	1.7	1.8	V
Pulled up Impedance Note(1)	R_{PWM_UP}	Controlled by EN & VCC_POR & VDRV_POR		19		kΩ

Pulled down Impedance Note(1)	R_{PWM_DOWN}	Always enabled		10		kΩ
Minimum PWM High/Low Pulse for Safe Operation Note(1)	$t_{PWM\_HI\&LO\_MIN}$	Requirement on controller PWM output	50			ns
Minimum PWM Tri-state Time for Safe Operation Note(1)	$t_{PWM\_TRI-STATE\_MIN}$	Requirement on controller PWM output	50			ns
GATEL Pull Down Resistance	R_{GL_PULLDN}	PWM=Tri-state	28	46	63	kΩ
HS minimum turn on time Note(1)	$T_{ON\_MIN\_HS}$	SW rising 10% to falling 10%		50		ns
LS minimum turn on time Note(1)	$T_{ON\_MIN\_LS}$	GATEL Rising 10% to falling 10%		50		ns
Current Sense Output-IMON						
Offset	A_{IMON_OFFSET}	0A load, R_{IMON}=1kΩ, 25℃	5		5	mV
Overall Accuracy Note(1)	A_{IMON_ALL}	0A~30A, R_{IMON}=1kΩ	-1.5		1.5	A
		30A~ 70A, R_{IMON}=1kΩ VIN=12V, VOUT=0.9V, 800kHz	-5		+5	%
GAIN	G_{IMON}	30A load, R_{IMON}=1kΩ, 25℃ VIN=12V, VOUT=0.9V, 800kHz	4.8	5	5.2	μA/A
REFIN Bias Current			-1	0	1	μA
IMON Propagation Delay Note(1)	t_{DELAY_IMON}	L=120nH, VIN=12V, VOUT=1.8V, Fsw=800kHz, IL Peak to IMON Peak		30		ns
Dynamic range of IMON Note(1)	V_{IMON}	TA = TJ = -40°C to 125°C, VCC = 4.5 V to 5.5 V, VIN = 4.5V - 16 V, REFIN=1.2V	0.8		VCC-2	V
Digital Input-EN						
Enable Power-on Delay	t_{DELAY_ENON}	PWM=0, Measured from EN rising edge to GATEL＞1V		10	13	μs
Enable Power-off Delay	t_{DELAY_ENOFF}	PWM=0, Measured from EN falling edge to GATEL＜4V		58	56	ns

Internal Pull-down Resistance	R_{EN_PULLDN}	EN is floating	360	460	557	kΩ
Input High Voltage	V_{EN_HIGH}		2			V
Input Low Voltage	V_{EN_LOW}				0.8	V
TMON/FLT-Temperature Sense Output and Fault Communication						
Temperature Sense Slope Note(1)	G_{TMON_SLOPE}	0°C＜Tj＜125 °C		8		mV/ °C
Temperature Sense Offset Voltage Note(1)	V_{TMON_OFFSET}	Tj=65°C，0.6V+8mV/ °C * Tj		1.12		V
TMON Source Current	I_{TMON_SOURCE}		436	575	714	μA
TMON Sink Current	I_{TMON_SINK}		14	20	25	μA
FLT Active High	V_{FLT_HIGH}	Over-Temperature, Over-Current, Bootstrap Undervoltage，or Phase Fault	3	3.3	3.6	V
FLT Active Low	V_{FLT_LOW}	No Fault, VCC＜UVLO			0.28	V
FLT mode Source Current	I_{FLT_SOURCE}	$V_{TMON/FLT}$=0V	4	4.6	5.2	mA
TMON Active Pull-down Resistance	R_{TMON_PULLDN}	No Fault, VCC＜UVLO	25	27	29	kΩ
Phase Fault Detection						
LS FET on, HS FET Short Threshold	$V_{HS\_FET\_FLT\_TH}$	VPHASE-VPGND higher than, GATEL＞1V		0.85		V
TMON/FLT Delay When HS FET Fault Note(1)	$t_{DELAY\_HS\_FLT}$	PWM High-Low Cycles to TMON/FLT high		1		cycle
HS FET on, LS FET Short Threshold	$V_{LS\_FET\_FLT\_TH}$	VIN-VPHASE higher than, GATEH-VPHASE＞1V		1.75		V

TMON/FLT Delay When LS FET Fault Note(1)	$t_{LS\_FET\_FLT}$	PWM High-Low Cycles to TMON/FLT high		1		cycle
Over-Temperature Protection						
Rising Threshold Note(1)	T_{RISE}	TMON/FLT pulled up high，Driver Temperature		140		°C
Falling Threshold Note(1)	T_{FALL}	TMON/FLT released Driver Temperature		120		°C
Cycle-by-Cycle Over-Current Protection						
Positive Peak Over-Current Threshold	I_{OC}			120		A
Positive Over-Current Hysteresis	I_{OC_HYS}			10		A
TMON/FLT Delay When OCP	t_{DELAY_OCP}	SW High-Low Cycles to TMON/FLT high Continuous 22 to report Continuous 3 to back		22		cycle
I Limit Comparator Input to Output Propagation Delay Note(1)	$t_{DELAY\_IMON\_COMP}$	Input Signal=200mV dv/dt=0.17mV/ns		60		ns
I Limit Blanking Time Note(1)	t_{BLANK_ILIMIT}	De-glitch filter (blanking) time for I Limit comparator trip		50		ns
Negative Over-Current Trip Low Level	I_{NOCP}	SW Low-High Cycles to TMON/FLT high		-50		A
INOCP_HYS Note(1)	NOCP Hysteresis			20		A
VCC and VDRV Under Voltage Lockout						
VCC Rising Threshold	V_{VCC_RISING}			4.1	4.4	V
VCC Falling Threshold	$V_{VCC\_FALLING}$		3.4	3.9		V
VCC Hysteresis	V_{VCC_HYS}			0.2		V

VDRV Rising Threshold	V_{VDRV_RISING}			4.2	4.5	V
VDRV Falling Threshold	$V_{VDRV\_FALLING}$		3.3	3.75		V
VDRV Hysteresis	V_{VDRV_HYS}			0.45		V
Bootstrap Refresh Off Threshold	$V_{BOOT\_REFRESH\_OFF}$			3.7	4.0	V
Bootstrap Refresh On Threshold	$V_{BOOT\_REFRESH\_ON}$		3.1	3.25		V
Bootstrap Refresh Hysteresis	$V_{BOOT\_REFRESH\_HYS}$			0.45		V
General						
VCC Supply Current Note(1)	I_{VCC}	VIN=12V, L=120nH EN=3.3V, PWM=800kHz, Duty=15%		5.4		mA
		VIN=12V, L=120nH EN=3.3V, PWM=500kHz, Duty=15%		5.4		mA
		EN=3.3V, PWM floating BOOT to PHASE=5V, SW short to GND	3.2	5	6.9	mA
		EN=0V, PWM floating BOOT to PHASE=5V, SW short to GND	38	65	92	μA
VDRV Supply Current	I_{VDRV}	VIN=12V, L=120nH, EN=3.3V, PWM=800kHz, Duty=15%		34.7		mA
		VIN=12V, L=120nH, EN=3.3V, PWM=500kHz, Duty=15%		21.7		mA
		EN=3.3V, PWM Floating，BOOT short to VDRV，SW short to GND	180	240	300	μA
		EN=0V, PWM Floating, BOOT short to VDRV, SW short to GND	129	184	240	μA

VIN Bias Current	I_{VIN}	EN=3.3V, VIN=15V, V(PWM)=1.65V, BOOT to PHASE=5V, SW short to GND	202	430	659	μA
		EN=0V, VIN=15V, V(PWM)=1.65V, BOOT to PHASE=5V, SW short to GND		34	112	μA
SW Floating Voltage	V_{SW_FLOAT}	V(PWM)=1.65V	1.2	1.4	1.7	V
SW Pull Down Resistance Note(1)	R_{SW_PD}	VCC=VDRV=0V	14.7	16	16.9	kΩ
BOOT to phase current	$I_{BOOT2PHASE}$	EN=3.3V, VIN=16V, V(PWM)=1.65V PHASE=16V, BOOT to PHASE=5V	179	235	291	μA
LSET						
LSET Output Voltage	V_{LSET}	LSET	1.05	1.2	1.35	V

Note:

(1) Guaranteed by design or bench characterization data, not tested in mass production.

9. Typical Performance Characteristics

Test conditions: VIN=12V, VCC=VDRV=5V, VOUT=1.8V, LOUT=120nH, Fsw=800kHz, TA=25°C and natural convection cooling unless otherwise specified.

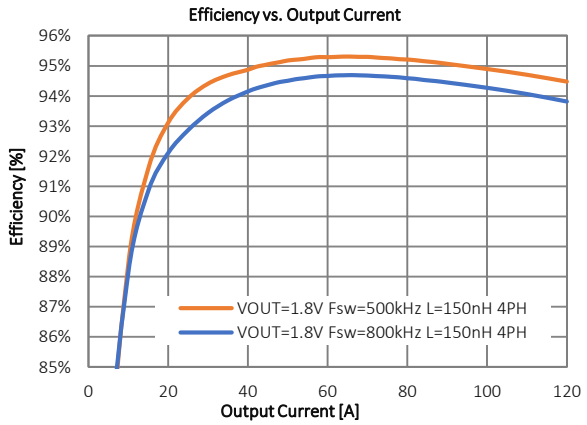


Figure 4. Efficiency Curve for 1.8V VOUT

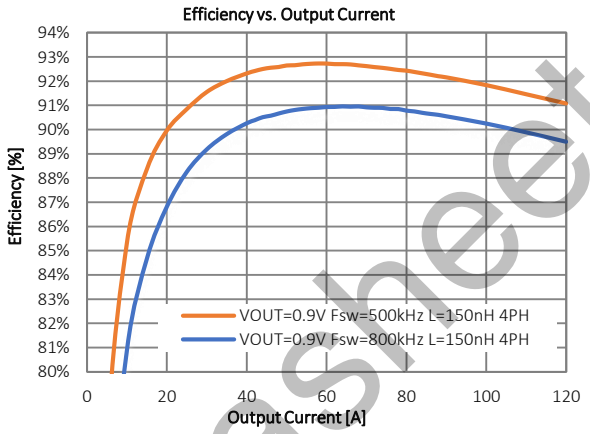


Figure 5. Efficiency Curve for 0.9V VOUT

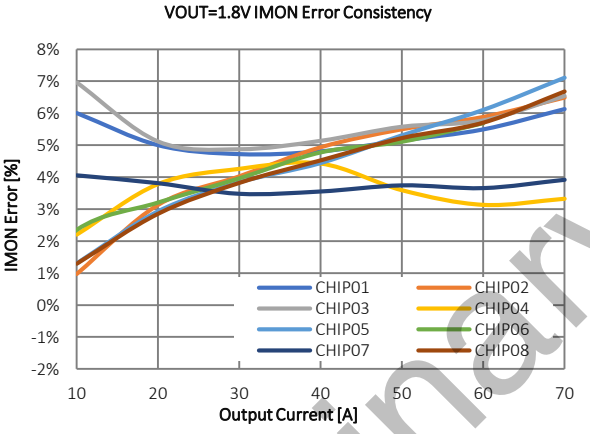


Figure 6. IMON Error Consistency VOUT=1.8V

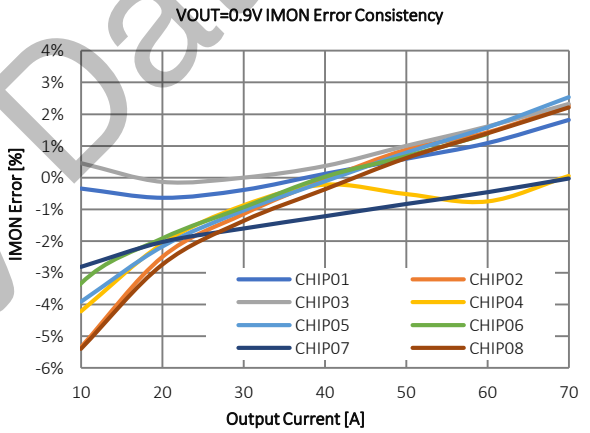


Figure 7. IMON Error Consistency VOUT=0.9V

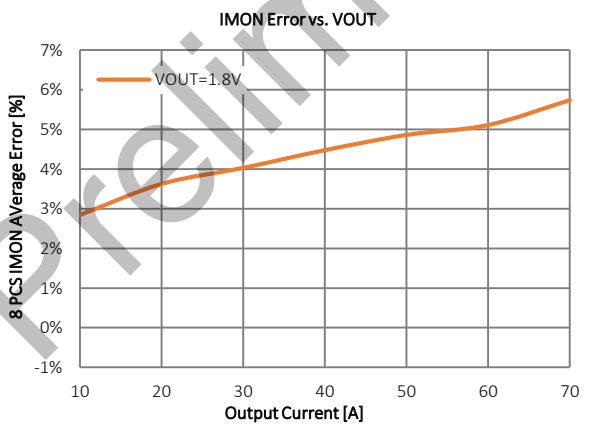


Figure 8. IMON Average Accuracy VOUT=1.8V

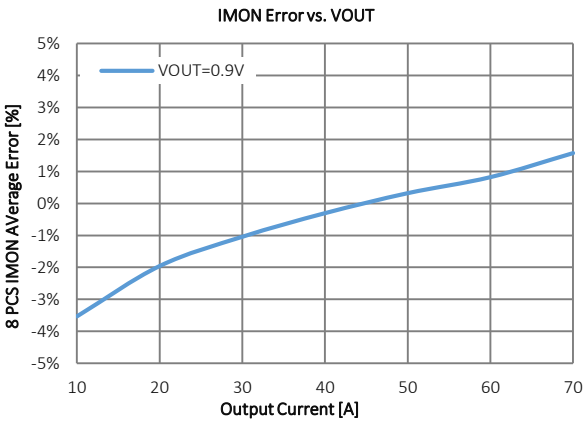


Figure 9. IMON Average Accuracy VOUT=0.9V

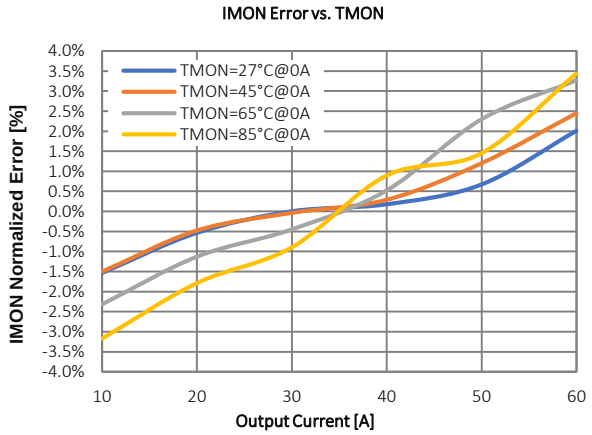


Figure 10. IMON Accuracy vs. Temperature

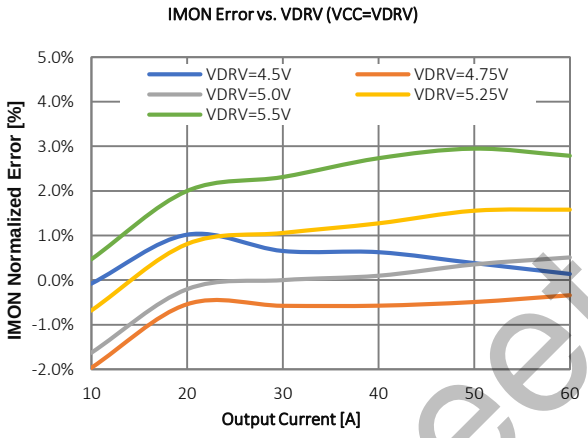


Figure 11. IMON Accuracy vs. VDRV

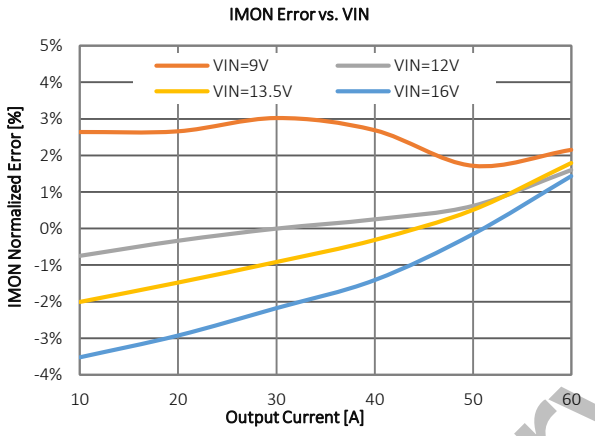


Figure 12. IMON Accuracy vs. VIN

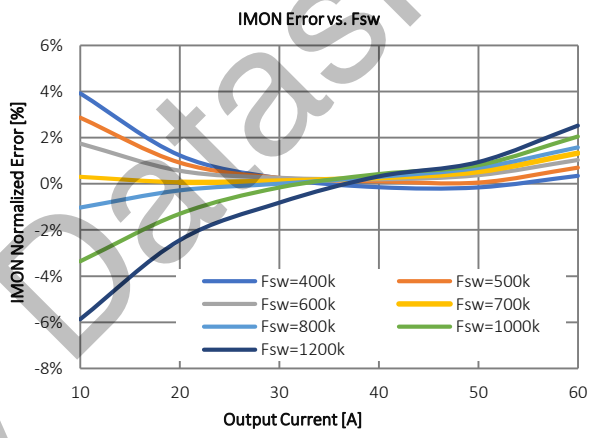


Figure 13. IMON Accuracy vs. Fsw

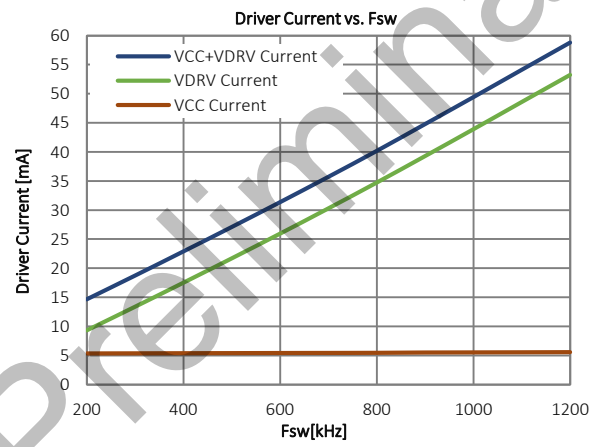


Figure 14. Driver Current vs. Fsw

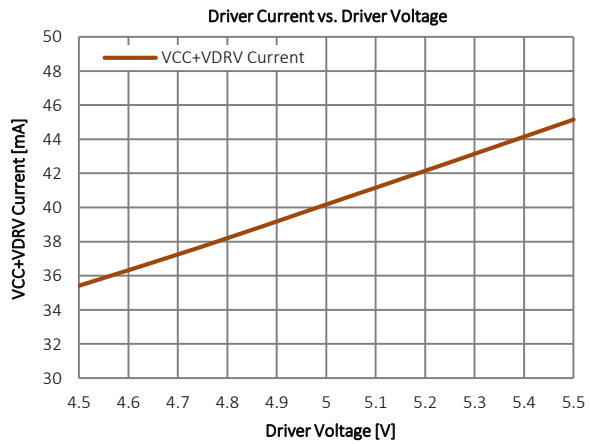


Figure 15. Driver Current vs. Driver Voltage

10. Block Diagram

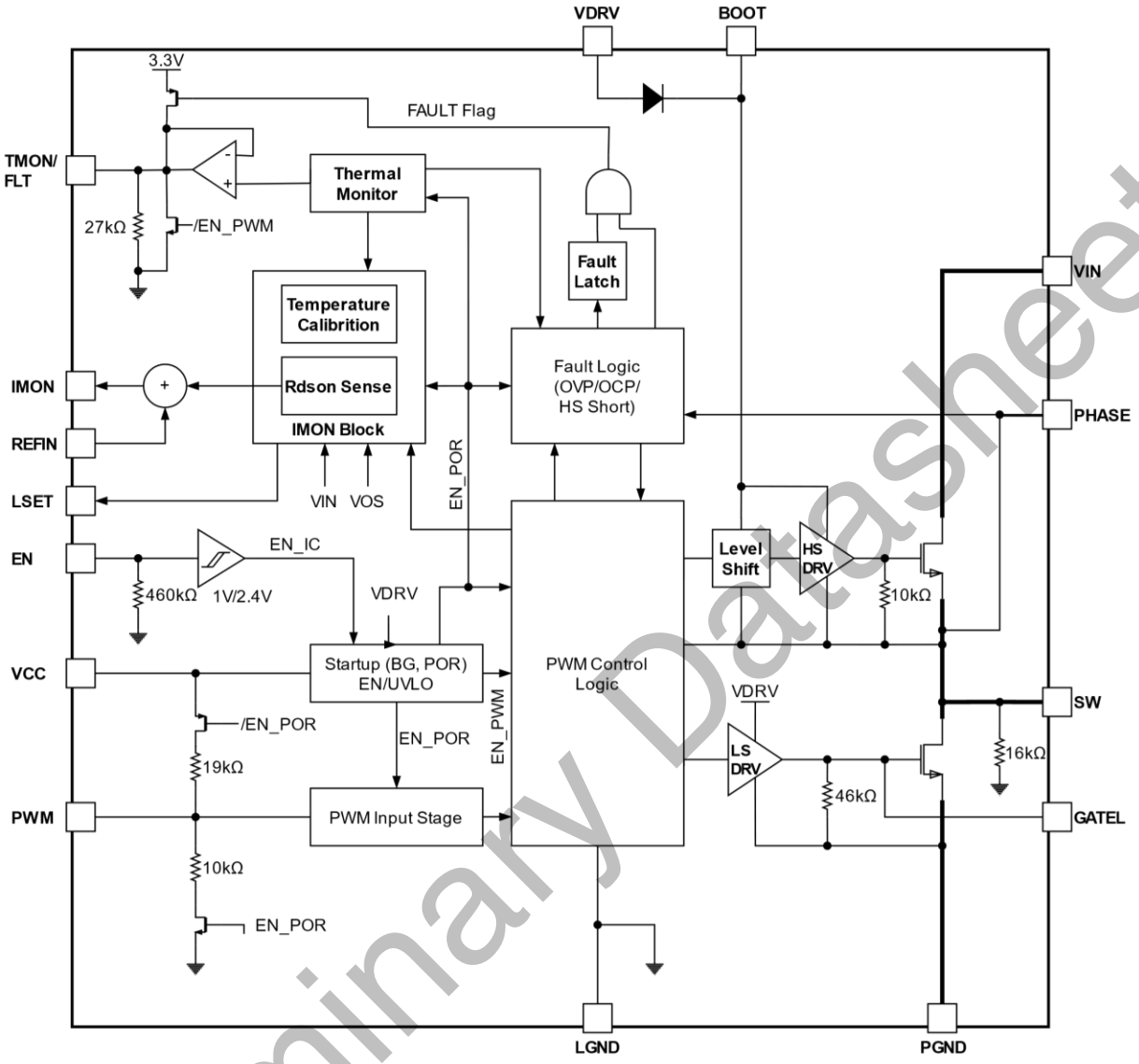


Figure 16. Functional Block Diagram

11. Operation

11.1 Startup & Shutdown

The PID3190A is enabled by both EN pin input signal and VCC/ VDRV/ BOOT-PHASE UVLO. During VCC UVLO, the driver is fully shutdown (GH, GL=0) and requires 50μs to startup. If VCC is ready and EN is low, the driver is partially shutdown (GH, GL=0) and requires 10μs to startup. If both VCC and EN are ready but VDRV and BOOT-PHASE UVLO, the driver analog circuitry being alive but outputs forced into Tri-state (GH, GL=0). When EN pin is open or pulled down by a PWM controller or an ASIC, the driver goes to sleep mode with very low quiescent current.

Table 1. UVLO and Driver Truth Table

VCC> UVLO	VDRV> UVLO	BOOT-PHASE> UVLO	EN	Driver State
0	X	X	X	Full driver shutdown (GH, GL=0), requires 50μs for startup;
1	X	X	0	Partial driver shutdown (GH, GL=0), requires 10μs for startup
1	0	0	1	Driver analog circuitry alive but outputs forced into Tri-state (GH, GL=0)
1	1	1	1	Enabled (GH/GL follows PWM)
X	X	X	Open/0	Disabled (GH, GL=0)

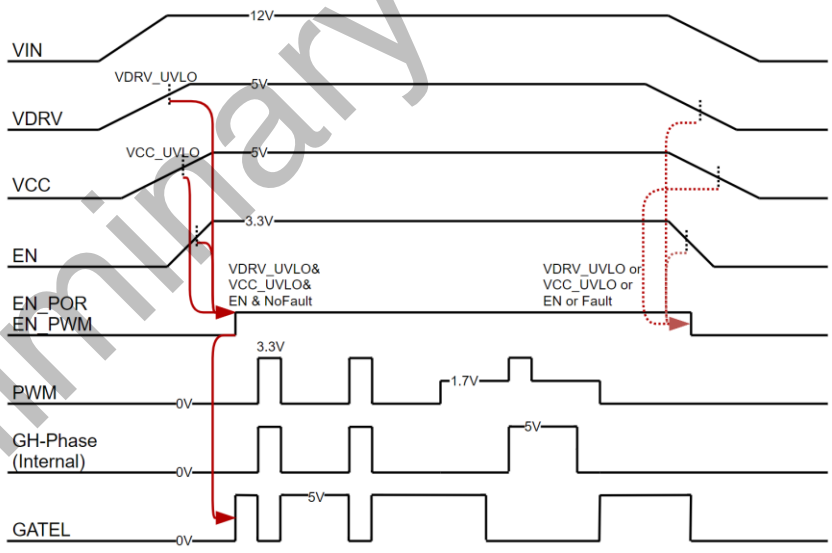


Figure 17. Startup and Shutdown Timing

11.2 Tri-state PWM Input

The PID3190A features a Tri-state 3.3V/5V PWM input gate drive design. The Tri-state gate drive has logic HIGH, logic LOW and a Tri-state shutdown window. When PWM input signal enters and keeps Tri-state for the defined hold-off time, both GH and GL are pulled low, so that both HSFET and LSFET are turned off, which helps to reduce output overshoot during load release or enter diode emulation mode to increase light-load efficiency. When load releases, multi-phase controller could discharge inductor current with a deeper slope (VOUT + Vdiode)/L, instead of VOUT/L, by sending Low - Tri-state PWM pulse. This reduces overshoot during large load release transient.

Table 2. Tri-state PWM Input Truth Table

EN	PWM	GH	GL
0	X	0	0
1	Tri-state	0	0
1	0	0	1
1	1	1	0

11.3 LSET Pin Function

Inductor value setting pin. After VCC is above UVLO, a 1.2V internal voltage source is applied to this pin, the output current is monitored to set inductor starting point for IMON reconstruction algorithm. The inductor value is set by 1kΩ/nH ratio. If the resistance is less than 10kΩ or short to GND，L=120nH (default) is set, if this pin is floating, L=210nH is set. The highest inductor value is 1.2uH. To get better IMON performance at startup point, it is recommended to use inductor value matching this calculation result. If not used, left this pin floating or short to GND.

11.4 Current Sensing and Reporting

The PID3190A integrates high accuracy current sense feature, which is based on low-side MOSFET drain source voltage (VDS) when it is on, and a synthesized current when high-side MOSFET is on. The driver incorporates build-in temperature compensation and inductance calibration for current sense to achieve high current sense accuracy and lower propagation delay. The reported current is in the form of current output and the gain is 5μA/A from the IMON pin. In order to convert this current into voltage, a 1kΩ, 0.1% resistor is recommended between PWM controller's ISEN and ISENREF pins and this resistor should be placed close to the PWM controller. In order to get a negative current reporting, it is not recommended to set ISENFEF to GND, but to a voltage between 1.1V and 1.9V. If the PWM controller ISEN sampling can accept a current signal, an external 1kΩ, 0.1% resistor is not required, and PID3190A IMON pin can be directly connected to the controller's corresponding ISEN pin. PID3190A REFIN pin can be left floating or can be connected to a voltage source between 1.1V and 1.9V.

11.5 Temperature Reporting and Over-Temperature Protection

PID3190A integrates an internal temperature detection circuitry. The sensed temperature is reported at the TMON/FLT pin with a linear voltage slope of 8mV/°C and a 0.6V offset at 0°C. TMON/FLT pin is also used as Faults indication pin, when positive over current protection (POCP), over-temperature protection (OTP), BOOT-PHASE UVLO, LSFET_SHORT or HSFET_SHORT occur, by pulling this pin up to 3.3V. When VDRV_UVLO occurs under power up or normal operation conditions, the TMON/FLT pin is weak pulled down to 0V (or VTMON from other Power Stages in same loop).

When the driver temperature rises higher than 140°C, the TMON/FLT pin will be pulled up to 3.3V and the driver will stop to respond to the controller's PWM. In this way, even if the controller doesn't latch-up and continues to send PWM, the MOSFETs will not switch to prevent the power stage from overheat and affecting long-term reliability. When the driver temperature drops below 120°C, TMON/FLT returns to the voltage value corresponding to driver detected temperature, and the driver starts responding to PWM again.

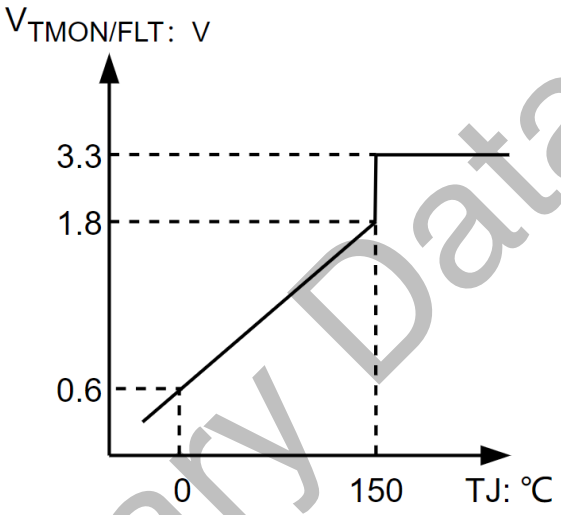


Figure 18. TMON/FLT

11.6 Positive Over Current Protection

PID3190A features Positive Over Current Protection (POCP) architecture by real-time sensing high-side MOSFET drain source voltage (VDS) when it is on. Once high-side MOSFET real-time sensing current exceeds the POCP threshold, a POCP event is asserted, and the PWM high pulse will be truncated after a short delay so that the high-side MOSFET peak current is almost equal to POCP threshold. If POCP is triggered for 22 consecutive SW cycles, the TMON/FLT pin is pulled up to 3.3V with the driver continuing to respond to PWM. When POCP is not triggered for 3 consecutive SW cycles, POCP event is de-asserted, and TMON/FLT returns to the voltage value corresponding to driver detected temperature.

PID3190A also features a POCP hysteresis circuitry and the typical threshold (I_{OC_HYS}) is 10A. In a PWM cycle, PWM is high and POCP is triggered, but when the PWM is low, the valley current value is greater than POCP- I_{OC_HYS}, then the next PWM high pulse from controller will be ignored and this kind of ignored PWM pulses will not be counted as POCP events. In other words, POCP assertion and de-assertion only counts the number of SW pulses.

11.7 Negative Over Current Protection

In some application scenarios such as DVID (Dynamic Voltage Identification) and OVP (Over Voltage Protection), the low-side MOSFET will be on for a long time to discharge the output energy. If the low-side MOSFET is left on for too long due to incorrectly optimized control loops, the power stage may be damaged because of inductor reverse saturation. Even if the inductor is not reverse saturated, when the low-side is off, this large negative current will pass through the body diode of the high-side MOSFET and may damage the body diode of the high-side MOSFET. In summary, NOCP is necessary.

PID3190A features a Negative Over Current Protection (NOCP) circuitry by real-time sensing low-side MOSFET drain source voltage (VDS) when it is on. Typical threshold is -50A. When the low-side MOSFET real-time sensing current reaches to -50A, the driver will force the low-side MOSFET to be off and high-side MOSFET to be on. But the driver will continue to respond to PWM and report current. There is also a NOCP hysteresis with a typical value of 20A. That is to say when negative current rises to -30A from -50A, low-side MOSFET will follow PWM levels. Note that NOCP event will not pull high or pull low TMON/FLT pin.

11.8 VDRV Undervoltage Lock-out (UVLO)

PID3190A integrates an VDRV UVLO circuitry to actively detect the voltage of the VDRV before power-on and during operation.

Before powering up, if VDRV voltage is below the UVLO threshold (Typical 4.2V), the PWM will be weakly pulled down to GND. This can be used as an indicator signal to tell the PWM controller that the PID3190A is still in VDRV UVLO status. As soon as VDRV voltage exceeds the UVLO threshold, the PWM voltage will change to Tri-state (typical 1.7V) from 0V, indicating that the PID3190A is ready for operation. At the same time, PID3190A will short IMON and REFIN to indicate that it is in UVLO condition.

In normal operation condition, if VDRV UVLO occurs, the device will stop switching. IMON pin, PWM pin and TMON/FLT pin will be pulled down to 0V. PWM pin and TMON/FLT pin are weekly pulled down to GND, so PWM pin voltage can be driven by controller but no switching on Power Stage, and If there are multiple phases connected in the same control loop TMON/FLT pin will continue reporting the highest device temperature.

11.9 Bootstrap Capacitor Under-Voltage Protection

PID3190A keeps monitoring the BOOT-PHASE voltage. If EN, VCC and VDRV are ready, but the voltage across the bootstrap capacitor voltage is lower than $V_{BOOT\_REFRESH\_ON}$ (Typical 3.25V), PID3190A ignores the PWM input signal and starts the boot refresh circuitry. The boot refresh circuitry turns on LSFET for 700ns every 8μs until BOOT-PHASE voltage is above $V_{BOOT\_REFRESH\_OFF}$ (Typical 3.7V). If the BOOT-PHASE voltage is lower than 3V, then TMON/FLT will be pulled up to 3.3V, IMON/FLT pin is pulled to GND and PID3190A latched up.

11.10 High-side MOSFET and low-side MOSFET Short Protection

This feature reports the damage of high-side MOSFET and low-side MOSFET through TMON/FLT pin. In high output current scenario due to poor output inductor selection or incorrectly optimized control loop, the inductor can be saturated in either the positive or negative direction, which can damage high-side MOSFET or low-side MOSFET.

This function is enabled after the VIN rises above 4V and disabled when VIN falls below 3.65V. When low-side MOSFET is on, the driver continuously monitors the VDS voltage of the low-side MOSFET, so that once this voltage is higher than $V_{HS\_FET\_FLT\_TH}$ (Typical 0.85V), the high-side MOSFET short event is asserted. When high-side MOSFET is on, the driver continuously monitors the VDS voltage of the high-side MOSFET, and once this voltage is higher than $V_{LS\_FET\_FLT\_TH}$ (Typical 1.75V), the low-side MOSFET short event is asserted. For both high-side MOSFET short and low-side MOSFET short events, TMON/FLT is pulled up to 3.3V in 1 PWM cycle, the driver continuous to respond to PWM commands with IMON pulled up to 3.3V.

11.11 Fault Reporting and Identification

PID3190A features rich protection functions and fault reporting by identification of combinations of PWM, IMON, TMON/FLT status, including:

- VCC_UVLO and disabled by EN
- VDRV_UVLO (Before power up and normal operation)
- Positive OCP (POCP, Peak and Valley)
- Negative OCP (NOCP, Peak and Valley)
- BOOT-PHASE UVLO & Refresh
- LSFET Short: HS on (Internal GATEH-PHASE>1V) and VIN-PHASE >1.5V
- HSFET Short: LS on (GATEL>1V) and PHASE-PGND>0.85V
- OTP

Table 3. Fault Reporting and Identification

Fault Name	Fault Description	Fault Response	PWM	IMON	TMON/FLT
VCC_UVLO or disabled by EN	VCC Undervoltage Lockout or disabled by EN pin	Shutdown, non-latching	High-Z	=REFIN By external circuits	High-Z
VDRV_UVLO (Power up)	Driver Undervoltage Lockout		Weak pull down to 0V (PWM pin voltage can be driven by controller, no switching on Power Stage)	=REFIN	Weak pull down to 0V (or VTMON from other Power Stages in same loop)
VDRV_UVLO (Normal operation)	Driver Undervoltage Lockout			=0V	
POCP (Sourcing) (Peak and Valley)	Peak positive SW current limit; HS FET not turn on if IL> I_{OC}- I_{OC_HYS}	Cycle-by-Cycle Clamp inductor peak current	Response to PWM	Continues reporting current	Assert: 22 cycles to asserted. De-assert: 3 OCP-free cycles
NOCP (Sinking) (Peak and Valley)	Negative overcurrent: peak negative current threshold that turn off the LSFET				Not asserted
BOOT_UVLO	Boost Supply Undervoltage Lockout BOOT-PHASE <3V	Ignore PWM and refresh BOOT capacitor, until BOOT-PHASE > 3.7V	Ignore PWM till BOOT_UVLO clear	0V when TMON asserted	Asserted and latch up if lower than 3V
LSFET_SHORT	HS on (GATEH-VPHASE>1V) and VIN-VPHASE > 1.75V	Continue to respond to PWM commands	Response to PWM	=3.3V High Priority	Asserted and latch up
HSFET_SHORT	LS on (GATEL>1V) and VPHASE-VPGND > 0.85V				
OTP	Over Temperature Protection	Shutdown, non-latching	Power Stage stops	REFIN	Asserted =3.3V

12. Application

12.1 Typical Application

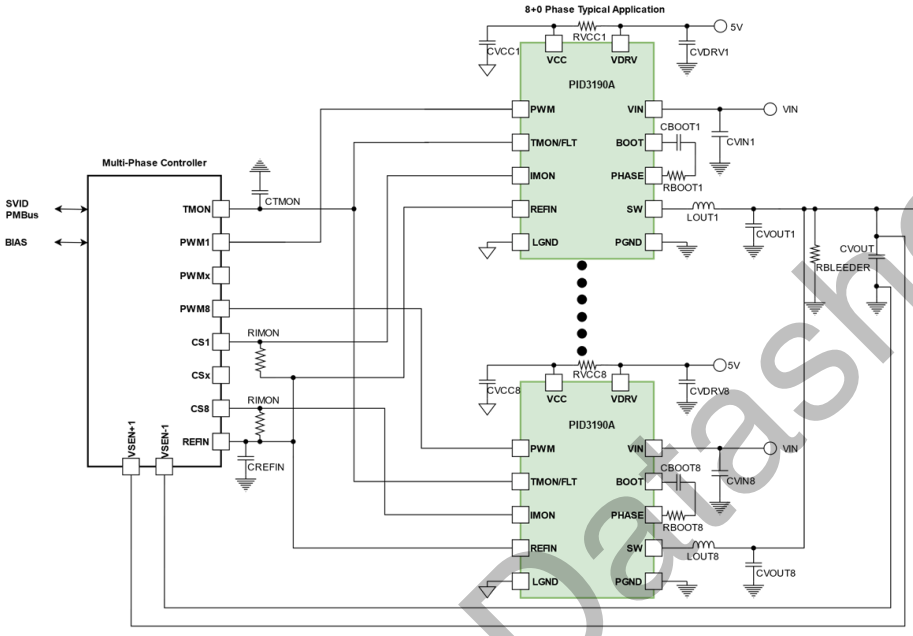
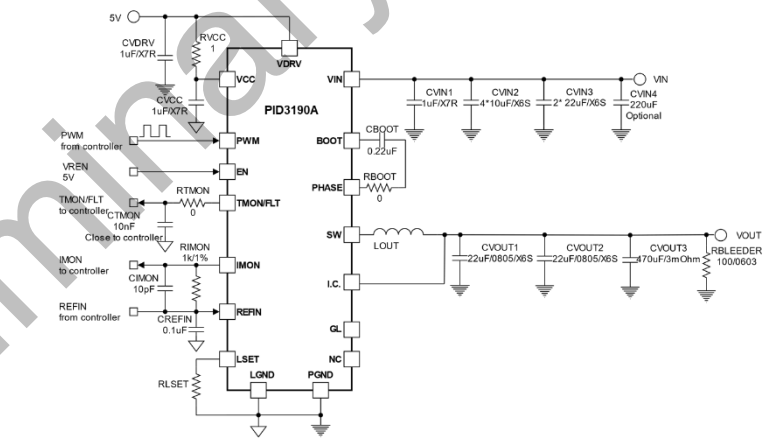


Figure 19. Simplified 8 Phase Schematic

12.2 Reference Schematic

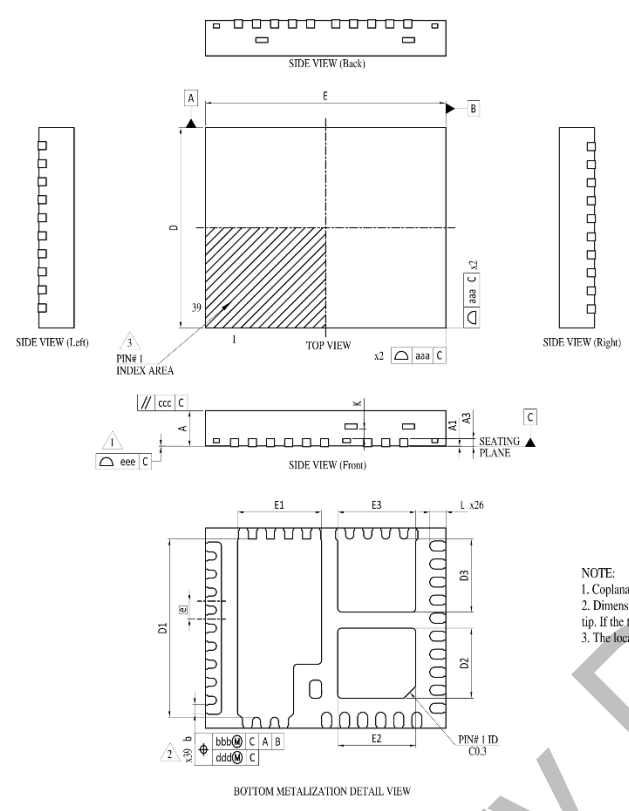


Note:
1. EN Pin(35) can connect with 5V directly.
2. Only one 10nF TMON/FLT capacitor is required and is placed close to controller when multiple TMON/FLT nets(Multi-Phase application) are connected together.
3. CIMON and RIMON are placed close to the controller, CIMON can be DEPOP if there is no HF-Noise between IMON and REFIN.
4. Only one 0.1uF REFIN capacitor is required and is placed close to controller when multiple REFIN nets(Multi-Phase application) are connected together.
5. Each output inductor is followed by 2 pcs 22uF/0805/X6S MLCC.
6. Only one RBLEEDER is required per VOUT net in both single and multiple phase application. When VOUT is higher than 2.2V(50% drating of PRBLEEDER), RBLEEDER package or resistance value may need to be changed.
7. For applications with VIN greater than 14V RBOOT change to 2Ω.

Figure 20. Reference Schematic with Notes

13. Mechanical, Packaging

13.1 Package Size



Dimensions: mm

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.203 Ref	---
b	0.20	0.25	0.30
D		5.00 BSC	
E		6.00 BSC	
e		0.45 BSC	
D1	4.35	4.45	4.55
E1	2.00	2.10	2.20
D2	1.65	1.75	1.85
E2	1.85	1.95	2.05
D3	1.725	1.825	1.925
E3	1.85	1.95	2.05
L	0.30	0.40	0.50
K	0.15	---	---
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTE:
1. Coplanarity applies to the terminals and all other bottom surface metallization
2. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.3mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
3. The location of the terminal #1 identifier is within the hatched area.

Figure 21. Package Size Information

13.2 Solder Resist

Dimensions: mm

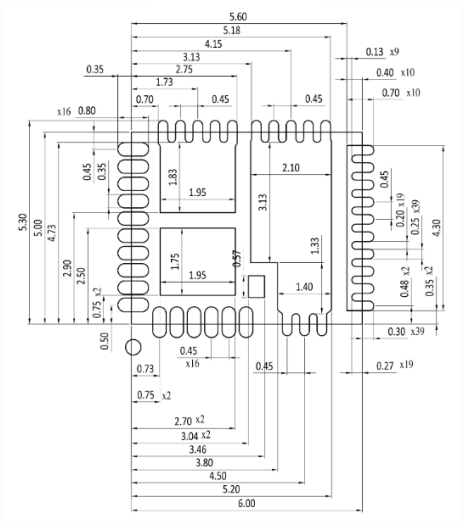
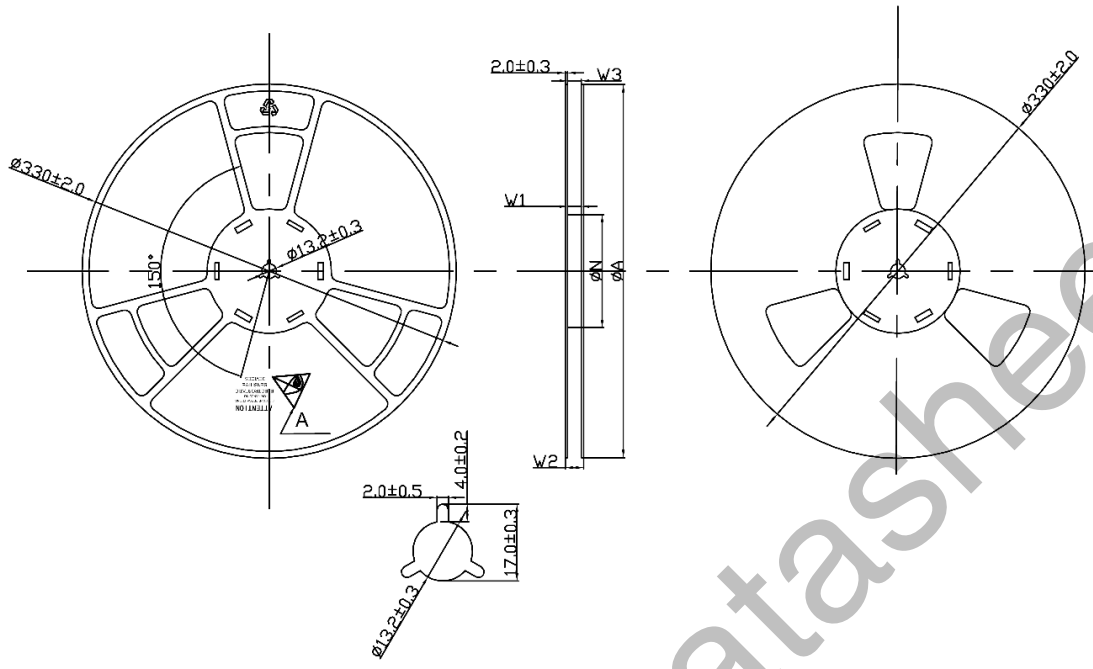


Figure 22. Recommended Solder Resist

13.3 Reel and Tape Information



Dimensions: mm

PRODUCT SPECIFICATIONS					
TYPE WIDTH	ØA	ØN	W1(+2/0)	W2(Max)	W3(Max)
12MM	330±2.0	100±1.0	12.4	18.4 ⚠	11.9/15.4

Figure 23. Reel Dimensions Information

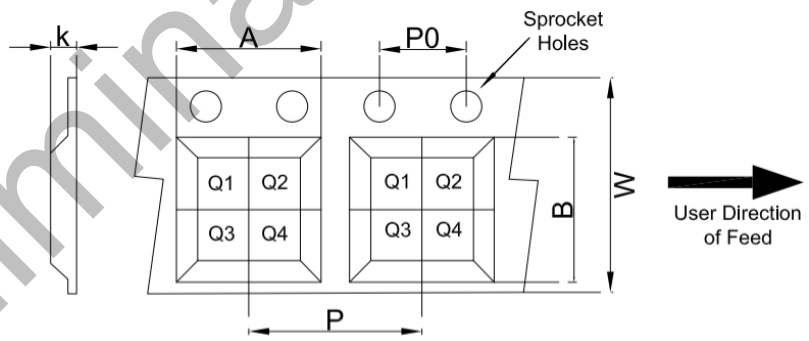


Figure 24. Tape Dimensions Information

Table 4. Tape Dimensions Information

Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
PID3190A	DFN5X6-39L	39	5000	6.3±0.1	5.3±0.1	1.2±0.1	8±0.1	8±0.1	12±0.3	Q2

13.4 Reel Box Dimensions

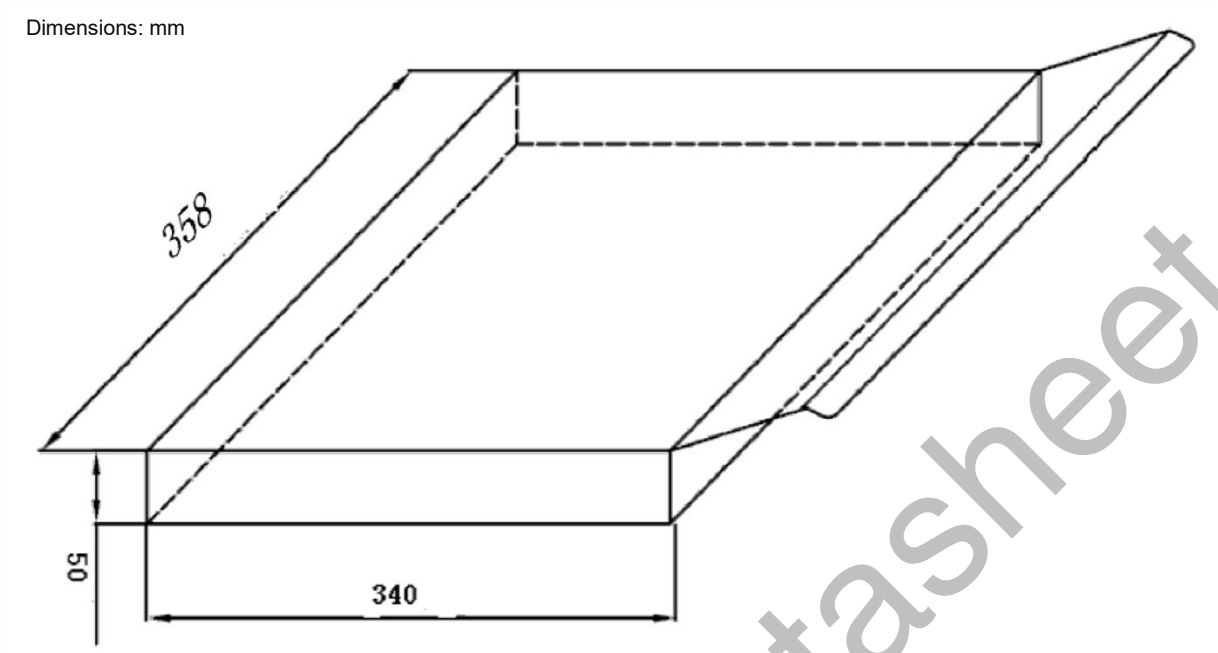


Figure 25. Reel Box Dimensions Information