

General Description

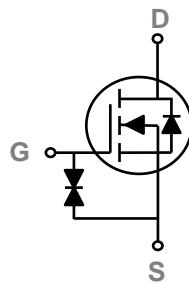
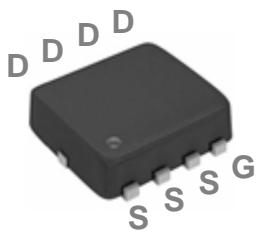
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

BVDSS	RDS(ON)	ID
20V	10mΩ	30A

Features

- 20V,30A, RDS(ON) =10mΩ @VGS = 10V
- Improved dv/dt capability
- ESD Protection Diode Embedded
- Green Device Available

PPAK3X3 Pin Configuration



Applications

- MB / VGA / Vcore
- POL Applications
- SMPS 2nd SR
- Li-Battery Protection

Absolute Maximum Ratings T_c=25°C unless otherwise noted

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	20	V
V _{Gs}	Gate-Source Voltage	±10	V
I _D	Drain Current – Continuous (T _c =25°C) (Chip Limitation)	30	A
	Drain Current – Continuous (T _c =100°C) (Chip Limitation)	19	A
I _{DM}	Drain Current – Pulsed ¹ (Chip Limitation)	120	A
P _D	Power Dissipation (T _c =25°C)	26	W
	Power Dissipation – Derate above 25°C	0.21	W/°C
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction to ambient	---	62	°C/W
R _{θJC}	Thermal Resistance Junction to Case	---	4.8	°C/W

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)
Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to $25\text{ }^{\circ}\text{C}$, $I_D=1\text{mA}$	---	0.02	---	$\text{V}/\text{ }^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$, $T_J=25\text{ }^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$, $T_J=125\text{ }^{\circ}\text{C}$	---	---	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 10\text{V}$, $V_{DS}=0\text{V}$	---	---	± 10	μA

On Characteristics

$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=4.5\text{V}$, $I_D=5\text{A}$	---	8	10	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}$, $I_D=3\text{A}$	---	9.5	12	$\text{m}\Omega$
		$V_{GS}=1.8\text{V}$, $I_D=2\text{A}$	---	12	17	$\text{m}\Omega$
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D = 250\mu\text{A}$	0.3	0.6	1	V
$\Delta V_{GS(\text{th})}$	$V_{GS(\text{th})}$ Temperature Coefficient		---	2	---	$\text{mV}/\text{ }^{\circ}\text{C}$
g_{fs}	Forward Transconductance	$V_{DS}=10\text{V}$, $I_S=5\text{A}$	---	12	---	S

Dynamic and switching Characteristics

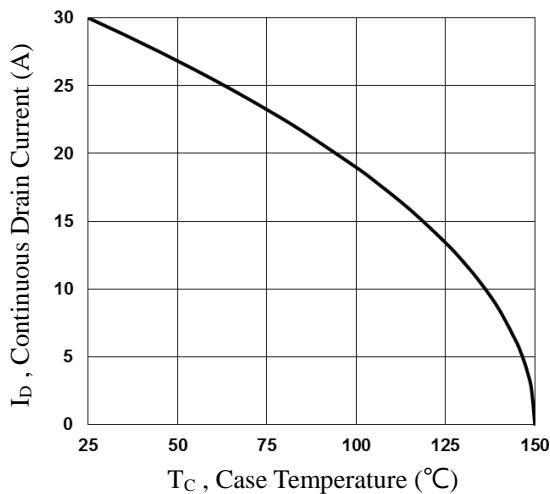
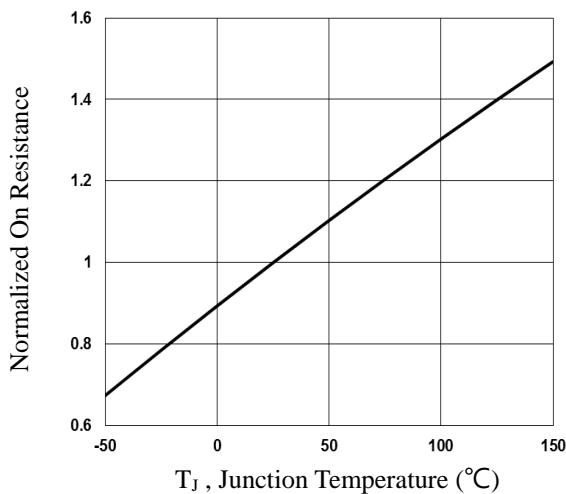
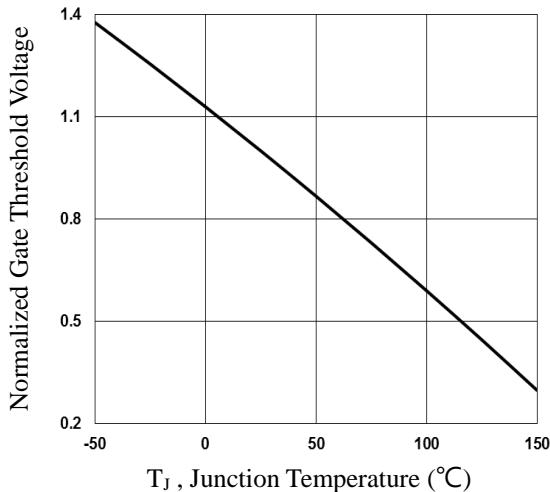
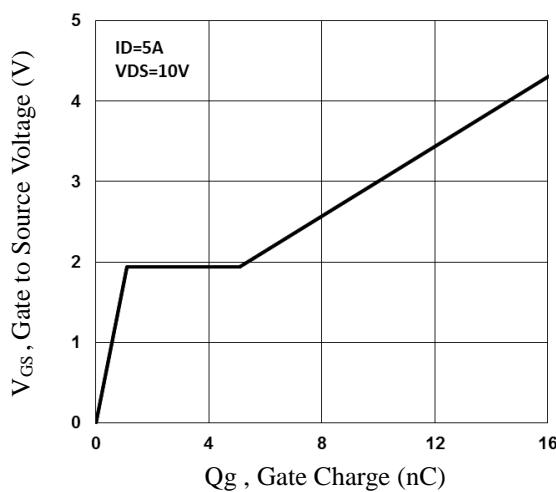
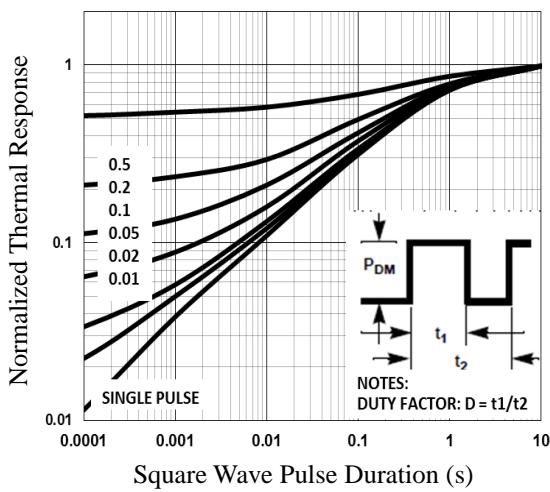
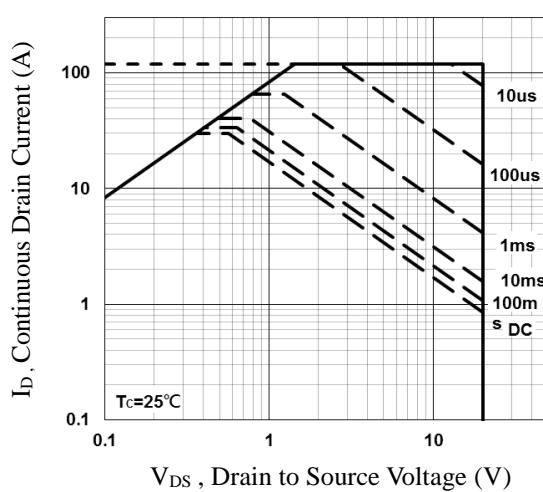
Q_g	Total Gate Charge ^{2,3}	$V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=5\text{A}$	---	16.9	26	nC
Q_{gs}	Gate-Source Charge ^{2,3}		---	1.1	3	
Q_{gd}	Gate-Drain Charge ^{2,3}		---	4	7	
$T_{d(on)}$	Turn-On Delay Time ^{2,3}	$V_{DD}=10\text{V}$, $V_{GS}=4.5\text{V}$, $R_G=25\Omega$ $I_D=1\text{A}$	---	6.8	13	ns
T_r	Rise Time ^{2,3}		---	20	38	
$T_{d(off)}$	Turn-Off Delay Time ^{2,3}		---	41.8	79	
T_f	Fall Time ^{2,3}		---	13.2	25	
C_{iss}	Input Capacitance	$V_{DS}=10\text{V}$, $V_{GS}=0\text{V}$, $F=1\text{MHz}$	---	1020	1480	pF
C_{oss}	Output Capacitance		---	160	240	
C_{rss}	Reverse Transfer Capacitance		---	110	160	
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $F=1\text{MHz}$	---	2	4	Ω

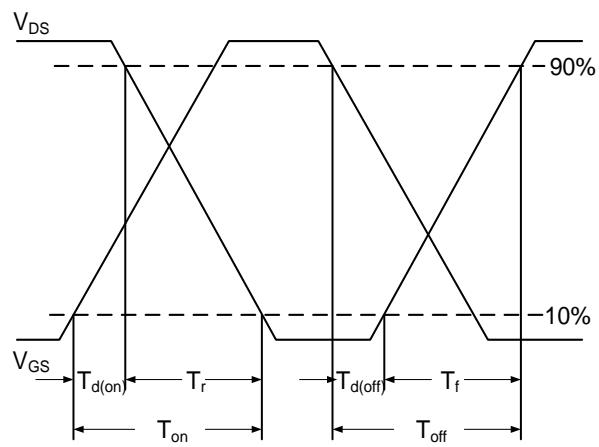
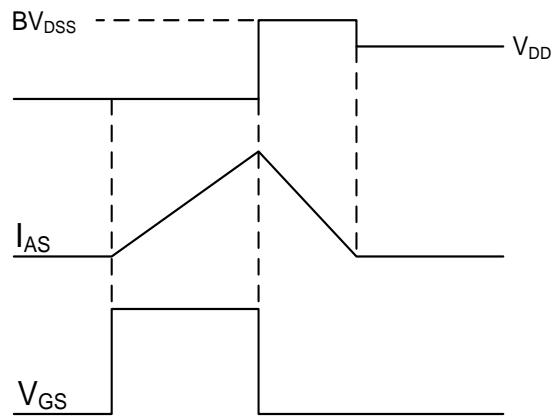
Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current	$V_G=V_D=0\text{V}$, Force Current	---	---	30	A
I_{SM}	Pulsed Source Current		---	---	60	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_S=1\text{A}$, $T_J=25\text{ }^{\circ}\text{C}$	---	---	1	V

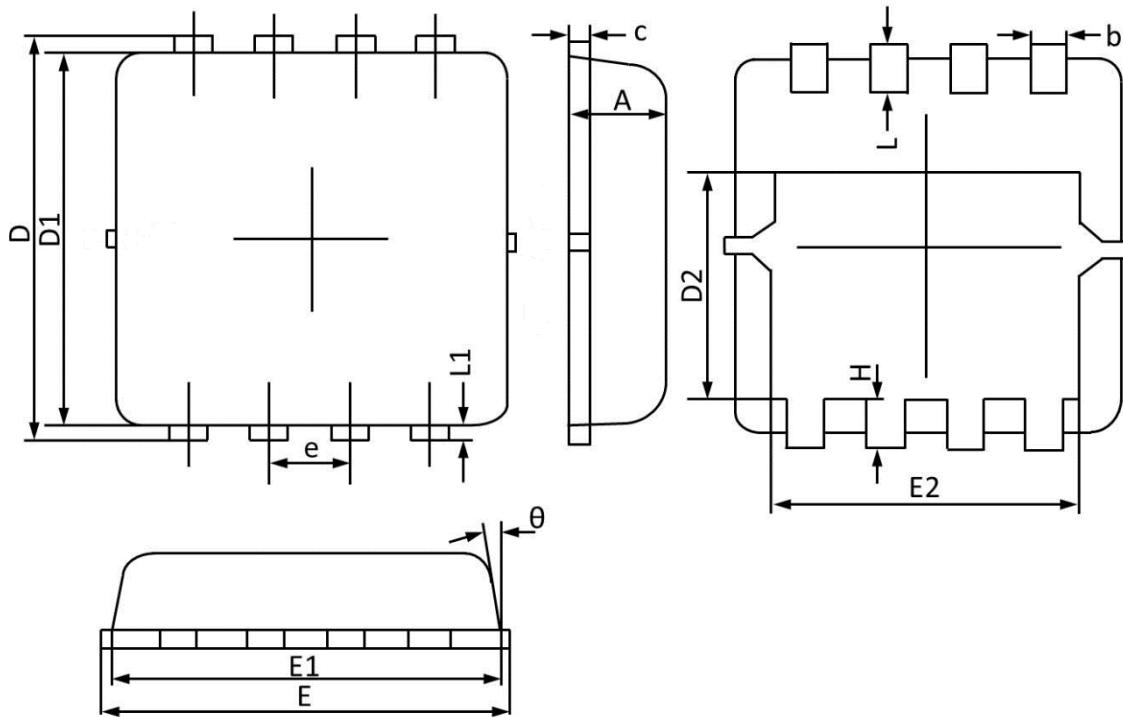
Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$.
3. Essentially independent of operating temperature.


Fig.1 Continuous Drain Current vs. T_c

Fig.2 Normalized RD_{SON} vs. T_j

Fig.3 Normalized V_{th} vs. T_j

Fig.4 Gate Charge Waveform

Fig.5 Normalized Transient Response

Fig.6 Maximum Safe Operation Area


Fig.7 Switching Time Waveform

Fig.8 EAS Waveform

PPAK3x3 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	0.900	0.700	0.035	0.028
b	0.350	0.250	0.014	0.010
c	0.250	0.100	0.010	0.004
D	3.500	3.050	0.138	0.120
D1	3.200	2.900	0.126	0.114
D2	1.950	1.350	0.077	0.053
E	3.400	3.000	0.134	0.118
E1	3.300	2.900	0.130	0.114
E2	2.600	2.350	0.102	0.093
e	0.65BSC		0.026BSC	
H	0.750	0.300	0.030	0.012
L	0.600	0.300	0.024	0.012
L1	0.200	0.060	0.008	0.002
θ	14°	6°	14°	6°

PPAK3X3 RECOMMENDED LAND PATTERN